Gate Centric Extended Source SOI TFET

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Abstract*: *An alternative SOI TFET structure precisely GCES SOI TFET has been proposed and studied in this paper by modifying its gate length for three different values. The proposed structure considering point and line tunneling has been derived and validated by simulation. The device is optimized to suitable V_{DS} of 0.1V, extended source alignment with the center position of gate and optimum drain contact position. The transfer characteristics, band diagrams, electric field and potential distributions are examined as the device performance parameter. The results distinctly exhibit that the device performs best when gate length is 10nm having SS as low as 19.8mV/dec and ratio of ON/OFF current as 10^{15}. SS increases and ON current decreases by a negligible scale when quantum confinement has been taken into account due to discrete energy band at the source channel interface using Schrödinger-Poisson model. The simulations are performed using Silvaco, Atlas. Moreover, the GCES SOI TFET inverter is characterized by SPICE calibration, provides a higher gain of 16 at lower V_{DD}=0.2V.

***Keywords*: *Ambipolar conduction, GCES-SOI TFET, inverter, subthreshold slope, Silvaco Atlas simulation, quantum confinement*.**

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I. INTRODUCTION

Tunnel Field Effect Transistors are promising devices for future that can supersede MOSFET [1]-[4] devices in terms of device performance and overcome the limitations posed by MOSFETs. TFET devices [5]-[8] can be modified achieve low power applications [9]-[12]. Also TFET devices fabrication can be integrated with CMOS process technology and therefore similar to MOSFET fabrication. Conventional TFET devices exhibit low ON current which can be improved by modifying the structures, device dimension, doping concentration etc. Si based TFET structures are advantageous over other new material [13]-[17] variations as they are consistent and can be integrated with CMOS processes. Thus novel TFET structures are developed in order to increase ON current of the device by enhancing tunneling area.

In the proposed work a trench gate SOI structure has been suggested along with source extension [18]-[19] and an intrinsic region at the lower portion of drain that works as LDD. The source extension increases tunneling area incorporating line tunneling along with point tunneling due to source gate overlap. Also the intrinsic region at the lower left portion of drain increases effective channel length. Hence, the possibility of depletion region to overlap with drain reduces and eventually results into greater ON current for the device.The lower left portion of the drain mirrors the extended source region in
opposite direction with low doping concentration to avoid the depletion region of both source and drain to overlap.

This overlap in low dimensional device may cause SCE like DIBL and to avoid the same such specific region variation has been considered. The gate length of the proposed structure has been varied and output characteristics have been examined by
performing simulation using Silvaco, Atlas. Simulations are performed considering with quantum and without quantum effects and a comparative study of the both has been presented in this work.

Source and gate overlap region creates modification in the understanding of tunneling at source and channel junction. The area covered includes line tunneling as well as point tunneling [20]-[21] at the mentioned interface.

When quantum effects [22] are considered in device operation, the conduction and valence energy bands no more remain continuous and become discrete spectrum of energy. Therefore tunneling will only be possible between the first energy states available for electrons and holes. This results into increase in tunneling width that causes reduction in BTBT probability along with reduction in ON current.

Going to implement any digital/analog application, the basic requirement is to design an inverter. But to comply the CMOS characteristics on a TFET, both N-TFET and P-Tfet should be designed properly by suppressing the ambipolar current for complementary performance [23-26]. In contrast, quantum simulation based approached is incorporated on the proposed GCES-SOI TFET n-type and p-type TFET to improve device ON current and suppress the ambipolarity. Moreover, GCES-SOI TFET inverter is simulated using SPICE calibration to evaluate its performance in circuit applications

In this paper, work is described in the following manner, at first the detail structural description along with device parameters are provided. In the following section simulation setup and the models used for simulations have been described. A comparative investigation of the outcome considering quantum and without quantum are presented in the next segment of this paper followed by the conclusion that has been achieved from the results.

II. Device Structures and Parameters

Gate Centric Extended Source SOI TFET structure has been considered in this work. The proposed structure shown in Fig. 1 has an extended source part which overlaps under the trench gate. Channel region is intrinsic and the effective channel length increases due to the LDD. Two different oxides namely HfO_2 and SiO_2 have been used as gate dielectric. As the proposed structure has a trench gate, therefore the dielectric covers three sides of the gate as shown in the Fig. 1 The source concentration of 10^{20} cm^{-3} whereas drain doping is of N type with concentration of 10^{17} cm^{-3}. The channel region as well as the lower left part of drain is kept intrinsic (10^{12} cm^{-3}). A P type substrate below the buried oxide (SiO2) layer is considered for the proposed SOI structure in order to ease the process of fabrication as well as to avail other advantages offered by SOI such as less parasitic capacitance, less leakage current, more firm and stable structure. The work function of gate of the device has been considered as 4.85eV.

The device has three variations in gate length specifically 10nm, 7nm and 5nm. For 10 nm gate, length source region has a dimension of 12 nm × 10 nm with an extended part of area 7 nm × 5 nm. The drain has a low-doped intrinsic segment at the lower left part with dimension of 2 nm × 5 nm whereas the upper part of this segment has higher doping concentration and dimension same as the lower one. The rest of the drain has a dimension of 10 nm × 10 nm. Channel starts from the left side of trench gate, goes underneath the gate till the low-doped intrinsic drain segment. Gate oxide SiO_2 is 2 nm thick and has a dimension of 2 nm × 2 nm at the left part of gate and 10 nm × 2 nm under the gate. HfO_2 on the other hand is present at the right of gate having dimension of 2 nm × 2 nm. The trench gate is 1nm deep and has a variation in length of 10 nm, 7 nm and 5 nm. The objective of this gate length variation is to investigate the suitable gate length for such small dimensional device structure.

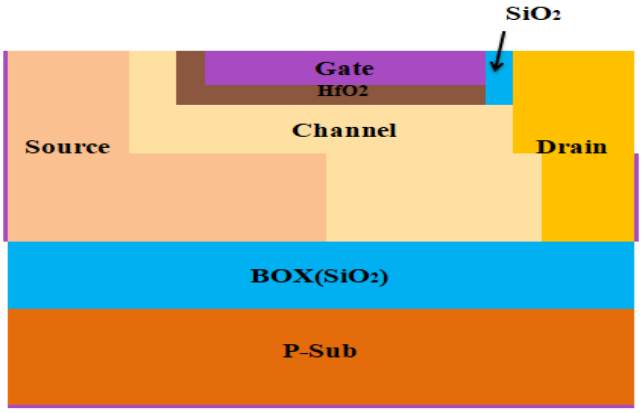


Fig. 1. Structure of Gate Centric Extended Source SOI TFET

Fabrication of the proposed device requires growing the structure layer by layer on top of silicon substrate. SiO_2 (BOX) layer can be grown on P type Si substrate by the method of oxidation. An intrinsic layer of Si is deposited on top of it. This layer is doped (left side P type for source and right side N type for drain) by the process of proper masking according to specific regions followed by diffusion of dopants. The same procedures of Si deposition, masking and diffusion could be carried out in accordance with specific region definition that would work as source, channel and drain. The channel region is then etched by photolithographic process and oxides (HfO2 and SiO2) are deposited in the etched area. The oxide is then etched according to its thickness required and gate metal is deposited in the etched area forming a trench gate structure. Source and drain contacts are at the two sides of the device along with one body contact below the substrate. Gate contact is taken from the top of the device on the gate metal. The fabrication steps are briefly illustrated in the Fig 2.

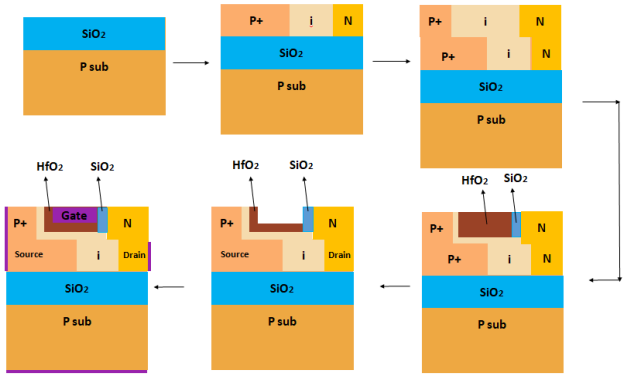


Fig. 2. Fabrication steps of the proposed structure

III. Simulation Setup And Model Descriptions

Silvaco Atlas based simulation has been performed considering quantum mechanical description along with quantization in sub-band transition using self-consistent Schrodinger Poisson model and classical model simulation that includes non-local BTBT, bandgap narrowing model, Fermi Dirac statistics, Auger and SRH (Shockley Read Hall) recombination models .

IV. Resuts And Discussions

In this section the outcome of the simulation considering classical behavior has been studied and the results in terms of transfer characteristics, band diagrams, electric field and potential along with contour diagrams are thoroughly investigated. Analytical current modelling which is performed in section IV has also been validated based on the simulation result in this section. Quantum confinement has been taken into account and the outcomes of the same is compared with the classical behavior for different gate length variations.

A. Optimum V_{DS}

The drain voltage of GCES SOI TFET has been varied for the gate length of 10nm. The subthreshold slopes are examined for three different V_{DS} values specifically 1V, 0.5V and 0.1V. The results found at different V_{DS} values are presented in the following Fig. 5. It is noticeable that 0.1V is optimum value for V_{DS} in this structure as it provides lowest SS.

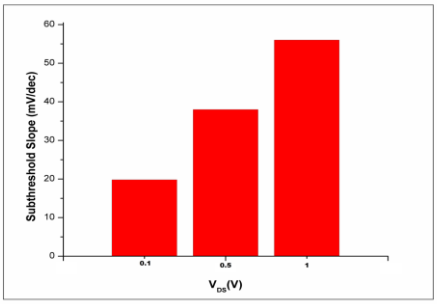


Fig. 5. Variation of V_{DS} for 10nm gate length of GCES SOI TFET Gate

B. Centric Source Extension

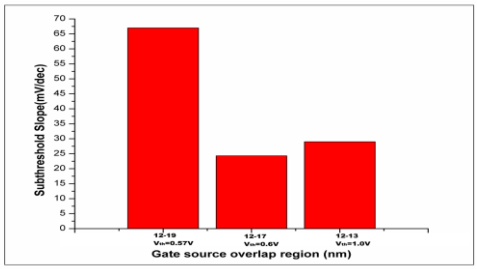


Fig. 6. Variation of gate source overlap region for 7nm gate length of GCES SOI TFET

From the comparison explained in the Fig. 6 it is evident that center position (12-17nm) of gate length is optimum for source
extension where both the threshold voltage and subthreshold slope are found to be suitable for device operation unlike for the other two cases where either the SS is high or the threshold voltage requirement is high which is not desirable.

Thus, we optimize the structure by taking V_{DS} as 0.1V and optimum source extension up to center position of gate for all the gate lengths of 10nm, 7nm and 5nm respectively.

B. Position of Source and Drain Contact

Drain and source contact positions have been varied and it is observed that specifically for drain contact position variation there is a change in subthreshold slope but the overall ON and OFF current are found to be similar whereas variation of source contact position does not create much impact on the device parameters. The variations are shown in Fig. 7.

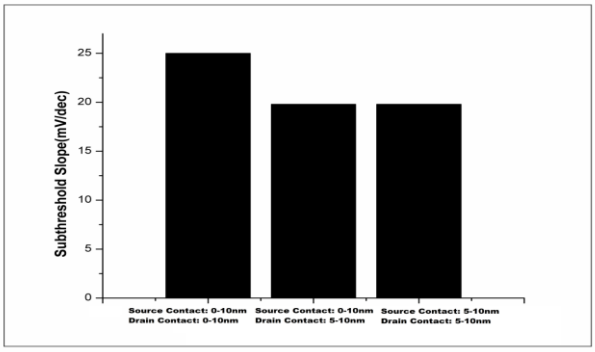


Fig. 7. Variation of drain and source contact position

C. Band Diagram

The energy bands for each of the gate lengths are compared and it is evident from the graph Fig8. that for 10nm gate length, tunneling is better at the source channel interface to some extent.

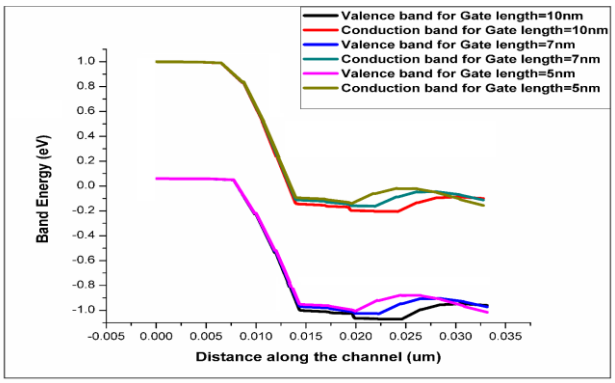


Fig. 8. Comparison of band diagrams of GCES SOI TFET for three different gate lengths of 10nm, 7nm and 5nm.

D. *Electric Field*

It is evident from the Fig. 9 that the electric field for 10nm gate length considering quantum and non-quantum is almost similar whereas for 7nm and 5nm gate length, electric field without considering quantum is higher than that of regarding quantum.

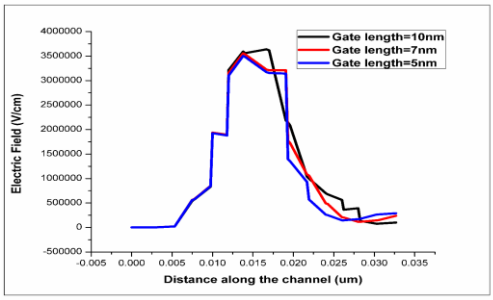


Fig. 9. Comparison of electric fields along the length of GCES-SOI TFET for three different gate lengths of 10nm, 7nm and 5nm.

E. *Surface Potential*

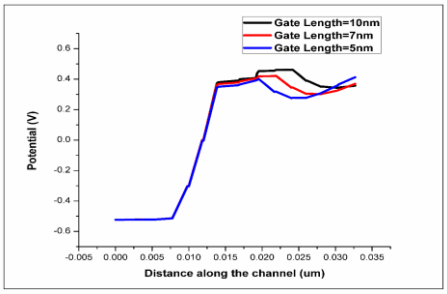


Fig. 10. Comparison of surface potential along the length of GCES-SOI TFET for three different gate lengths of 10nm, 7nm and 5nm.

In Fig. 10 the three graphs depict almost similar results for quantum and without quantum effects. In all the three cases potential of the proposed structure without considering quantum confinement has larger value of surface potential than the quantum effects.

F. *Transfer Characteristics*

It is evident from the Fig.11 that the curves differ from each other due to variation of subthreshold slope while the ON and OFF currents remain the same. Thereby establishing the superiority of 10nm gate length

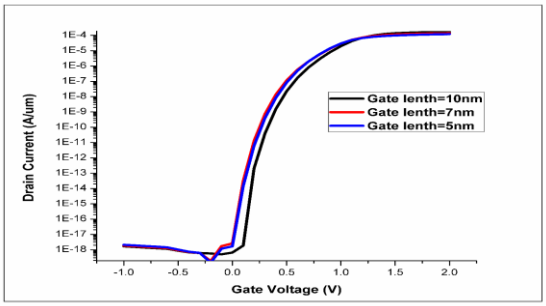
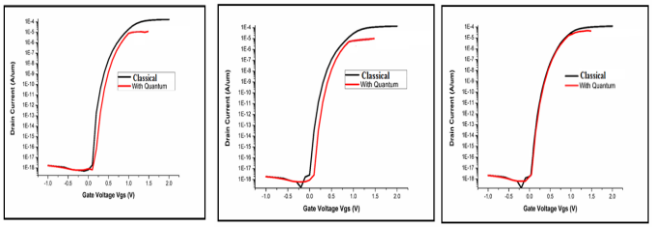


Fig. 11. Transfer Characteristics for GCES SOI TFET for gate lengths of 10nm, 7nm and 5nm.

V. Quantum Confinement

In this section quantum confinement due to low dimensional device structure has been considered and outcomes of the same have been comparatively studied with results of classical behavior.

A. *Transfer Characteristics*



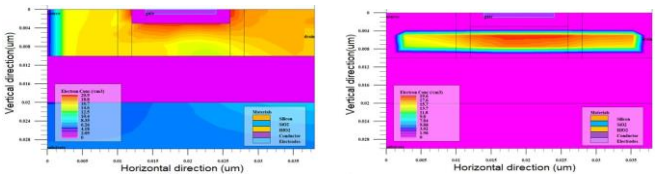
(a) (b) (c)

Fig. 13. Comparison of Transfer characteristics of GCES SOI TFET with considering quantum effects and classical behavior for three gate lengths of (a)10nm, (b)7nm and (c)5nm.

It is evident from the Fig. 13 that for three different gate lengths the ON current is higher (10^{-4} A/um) for classical approach that for quantum approach. The reason behind lower ON current for quantum confined results is the discretization of the energy bands at the source channel interface and thus the electrons can only tunnel through the first available empty energy state between the interfaces. There is no ambipolar conduction in all the cases taken into account and thus the device has the capability for low power applications. All the curves indicate the comparative performance between classical and quantum models.

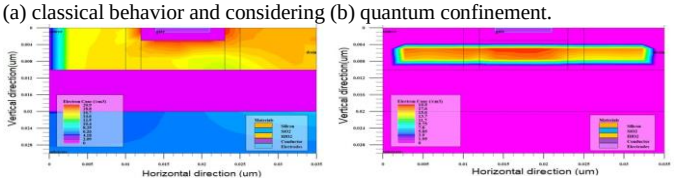
B. *Electron Concentration*

Electron concentration area within the device for quantum and without quantum are different. It is illustrated and clearly



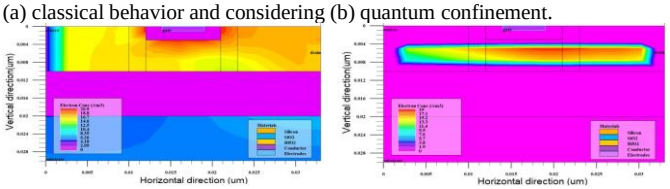
(a) (b)

Fig. 14. Electron concentration for 10nm gate length of GCES SOI TFET for (a) classical behavior and considering (b) quantum confinement.



(a) (b)

Fig. 15. Electron concentration for 7nm gate length of GCES SOI TFET for (a) classical behavior and considering (b) quantum confinement.



(a) (b)

Fig. 16. Electron concentration for 5nm gate length of GCES SOI TFET for (a) classical behavior and considering (b) quantum confinement.

visible from the contour diagrams that for all the three gate lengths of 10nm, 7nm and 5nm, electrons are confined within a particular area when quantum confinement has been considered whereas this confinement of electrons are absent in case of the same structures without quantum effects. The contour diagrams for the same are presented below in Fig 14, 15 and 16.

C. *Comparison of Subthreshold Slope*

The SS for three different gate lengths such as 10 nm, 7 nm and 5 nm have been compared and illustrated in the following Fig 17 where it is prominent that SS with considering quantum confinement is less on than that of classical behavior.

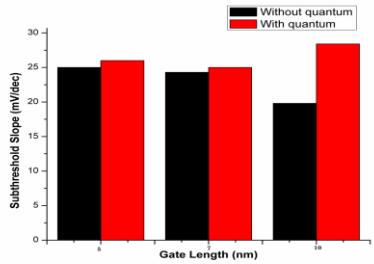


Fig. 17. Comparison of SS for gate length of 10nm, 7nm and 5nm of GCES SOI TFET.

VI. CONCLUSION

A GCES-SOI TFET with three different gate lengths are compared considering quantum confinements with that of neglecting quantum effects. The device is optimized with extended source part aligned with center position of the gate, drain contact position at the lower part of vertical dimension to the right side along with optimized V_{DS} value of 0.1V. The device transfer characteristics, electric field, potential distributions, band diagrams are extensively investigated and compared for different gate lengths. The comparative outcomes conclude that the 10 nm gate length structure is optimum for improved device performance in terms of parameters like SS, V_{th} and I_{ON}/I_{OFF} ratio. Considering quantum confinement it was evident that the device ON current decreases along with increase in SS due to discretization of the energy bands. The device can be adopted for both n-type and p-type devices for a the inverter implementation. The inverter has a higher voltage gain of 16 at V_{DD}=0.2V, has a high potential for future low power applications.

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