TCAD based modeling and simulation of Graphene Nanostructured FET (GFET) for High Frequency Performance

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Abstract:*In this paper, the modeling of a Graphene based Field Effect Transistor(GFET) is presented. The modeling is done using the SILVACO TCAD tools. The structure is developed in ATLAS virtual framework and the model is used to investigate the performance of graphene based FET. First we deposit 5nm thick polysilycon film instead of graphene film to generate the device structure. Graphene is modeled as a semiconductor, a carrier mobility of 10,000 cm^2/V-s and used as the channel material. The characteristics curves: output characteristic and transfer curve are plotted using TONYPLOT. Pristine graphene has no band gap. So it is considered as semi-metal or zero bandgapsemiconductor. Due to the lack of bandgap, I_{ON}/I_{OFF} is relatively low compared to the Silicon based transistor, so for digital logic circuits, GFET still lags behind comparing to Si transistors. It is more suitable for RF application with its very high mobility. Therefore, in this paper, the parameters which are considered to the FOMs of RF transistors i.e. maximum cut off frequency (f_T) and the maximum frequencies of oscillations (f_{max}) are extracted.*

Keywords:GFET, Graphene, ITRS, FoM, SILVACO, TCAD

1. Introduction

Transistor is the fundamental component of all the modern electronic circuits. Today, Si MOSFETs of 20nm gates are in mass production and in 2020 the International Technology Roadmap for Semiconductors (ITRS) requires 7.4 nm MOSFETs [1]. But silicon has the physical limitations of not being able to exist in the crystalline form below 10nm thickness. So, recently the search for technology beyond Si technology is going fast forward. Graphene has been considered as one of the probable substitute following Moore's law and the advancement in technology which demands the continual downsizing of device size. The aim of this paper is to model a structure and characterization of GFET using TCAD.

The energy band diagram of graphene shows no band gap. Due to the lack of bandgap, it shows a weak I_{ON}/I_{OFF} ratio which is not suitable for digital logic devices [1-4]. But considering its high electron mobility, it is quite suitable for RF devices which don't need to switch off. In 2009, 350 nm gates and a cut off frequency of 50 GHz; 240 nm gates with cut off frequency (f_T) =300 GHz in 2010 has been reported. Finally in 2012, graphene, MOSFET with the gate length 40nm and f_T =350 GHz [3]. In this paper, considering the suitability in the application of RF devices, we mainly focus on the study of some of the important figure of merits(FOMs) of RF devices like maximum cut-off frequency f_T.

2. GFET simulation

2.1 Methodology

ATLAS designs the GFET structure and predicts the electrical characteristics associated with specified bias conditions. ATLAS is a physically-based device simulator. Physically-based device simulators predict the electrical characteristics that are associated with specified physical structures and bias conditions.

2.2 Mathematical modeling

Basically, we need the following models for developing a MOSFET structure, viz. Shockley-Read Hall recombination (SRH), CVT or Lombardi model and

Boltzmann Transport Equation (BTE) [5]. Those models respectively describes the recombination-generation when the semiconductor attempts to return to the equilibrium state under disturbance, terminal current calculation as a function of carrier mobility in the inversion layer and the bulk of semiconductor and the electronic transport.

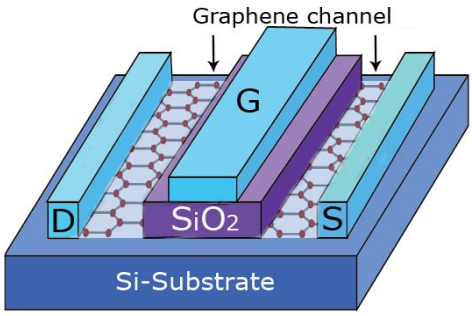


Figure 1: Proposed Structure of GFET

Several models can be used to demonstrate the recombination-generation process. The current flow depends upon the generation and recombination within the highly purity region. When semiconductors are under continual excitation whereby n and p are disturbed from their equilibrium states n_0& p_0, Shockley-Read Hall recombination which is known as SRH recombination is commonly used [5]. It is modeled as below:

$$R_{SRH} = \frac{np - n_i^2}{t_p(n+n_0)+t_p(p+p_0)} \quad (1)$$

The accuracy of the results of the calculation of terminal equation of 2D and 3D simulation depends on the carrier mobilities. Several mobility models for numerical device simulation exist in literature. But CVT model or Lombardi model is widely used for its accuracy. Then, the model is built by considering the following points. 1) Following the Matthiessen rule, 2) Thornber's scaling law, 3) including the impurity concentration, 4) parallel electric field and temperature effect. The transverse field, doping dependent and temperature dependent equation is given by CVT equation which is modeled as below:-

$$\frac{1}{\mu_r} = \frac{1}{\mu_{ac}} + \frac{1}{\mu_b} + \frac{1}{\mu_{sr}} + \frac{1}{\mu_{coulomb}} \quad (2)$$

The transport characteristic of GFET can be explained by Boltzmann transport equation (BTE). It is a limitation of Fermi-Dirac statistics when $(\varepsilon - E_F) >> kT_L$ resulting to:

$$f(\varepsilon) = \exp\left(\frac{E_F}{kT_L}\right) \quad (3)$$

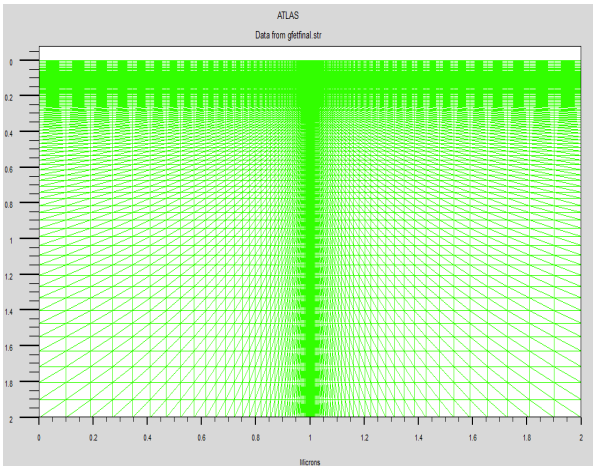
which is the probability $f(\varepsilon)$ that an that an available electron state with energy ε is occupied by an electron at temperature T_L where k is the Boltzmann constant and E_F is the Fermi energy.

2.3. TCAD modeling and simulation of the structure:

As mentioned above, the structure will be developed using ATLAS. Fig.3 shows the simulated structure of the proposed model. The graphene layer which is to be used as the channel layer is deposited over the SiO2 layer. Since graphene material is not yet included in the library of any simulator [6], so we have to take another material for graphene and redefine the parameters required later [5]. In our work, we chose the polysilicon. Table 1 shows the parameter of graphene required for using in MOSFET devices. If we accurately design the structure, we will get a correct and accurate electrical characteristic. So, 90% of our designing time must be devoted to modeling of the structure. Table.2 lists the design requirements to model the structure. The channel doped as p-type $1.0x10^{16}$ cm^3 and the source/drain as heavily doped n-type $1.0x10^{20}$ cm^3. The structure has been calibrated to meet the requirement of international technology roadmap for semiconductors (ITRS) [7] for the specific physical gate length.

TABLE 1 MATERIAL PARAMETERS OF GRAPHENE USED TO MODEL FET[2] [9] [15]

Parameters	E_G (eV)	χ	μ_n(cm^2 /V-s)	μ_p(cm^2 /V-s)	X (kg/mole)	v_{sat}
Description	Band gap	permittivity	Electron mobility	Hole mobility	Affinity	Electron saturation velocity
Value	0	25	10,000	10,000	4.248	$4x10^7$



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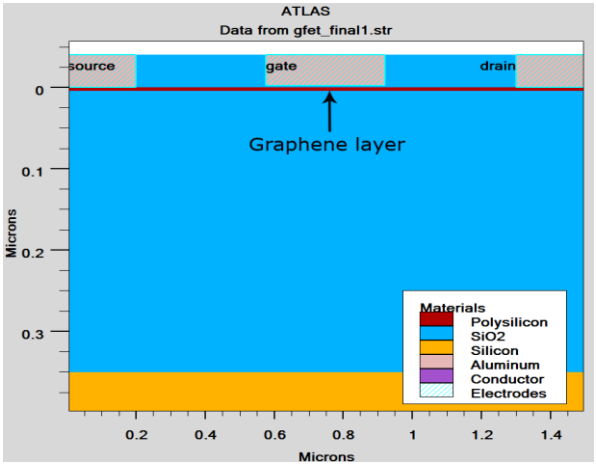


(b)

Figure 2: (a)Mess structure of the GFET model (b) Simulated model.

conditions for device simulation. The RF performances are studied and analyzed through AC analysis and s, y or h parameter extraction using S.PARAM, Y.PARAM OR H.PARAM respectively.

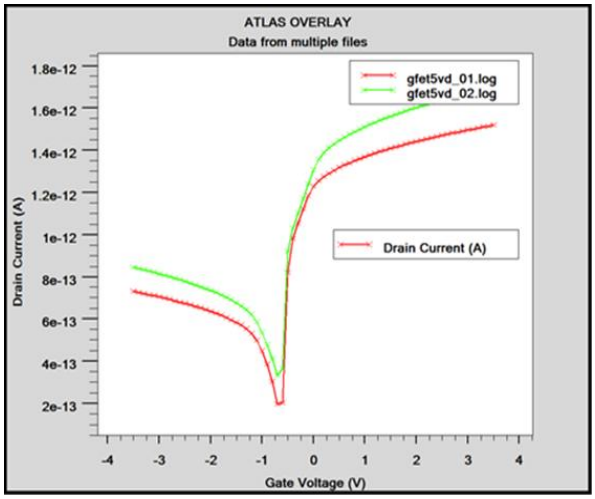
TABLE 2. DESIGN PARAMETERS OF THE PROPOSED MODEL

Parameters	Gate length (L)nm	Dielectric thickness(nm)	Channel doping (cm^3)	Source/drain doping (cm^3)	Substrate doping (cm^3)
Value	350	5	$1x10^{15}$	$1x10^{20}$	$2x10^{15}$

3. RESULTS AND DISCUSSION

3.1 I-V characteristics

Figure 3(a) shows the simulated transfer characteristics of the 350-nm gate graphene FET (GFET) for a drain-source voltage V_{DS} of 0.1 V and 0.2 V. The transfer curve (I_{DS}vs V_{GS}) for V_{DS}= 0.1V and V_{DS} = 0.2 volt with the gate voltage V_{GS} ramped from -3.5 to +3.5 V. The curve, as shown in fig.3 shows second linear region as expected from the experimental and theoretical reviews [1][4]. The output shows the predicted behavior of the device [11][12]. The output curve for different gate length is analyzed for both positive and negative values of V_{GS} to study the behavior of property of graphene channel to change the conductivity from n to p-channel and vice versa[8], and V_{DS} is ramped from 0 to 3.5 with V_{STEP}= 0.1 V.



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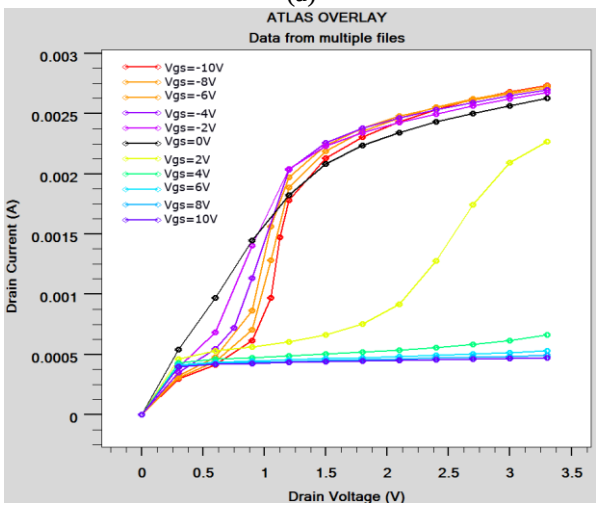
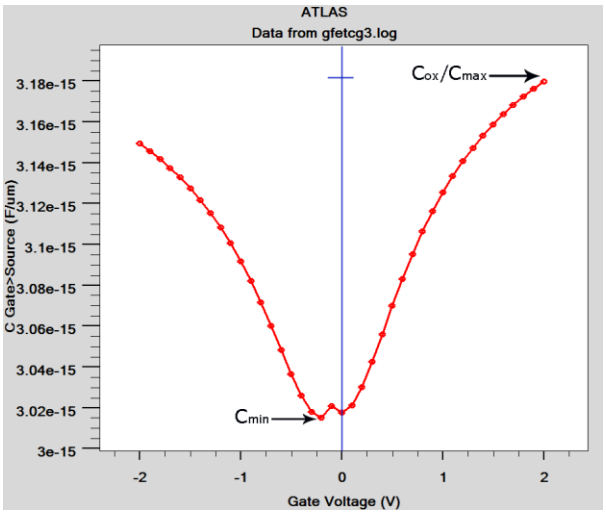


(b)

Figure 3: I-V curves of the device simulation (a) Transfer Curve (b) Output characteristics

3.2 RF parameters

The important high frequency or RF circuit parameters, FoMs are cut off frequency (f_T), transconductance and maximum cut off frequency[1] [8][10]. The intrinsic capacitances (gate to source capacitance, C_{GS} and gate to drain capacitance, C_{GD} as a function of V_{GS} for sub-threshold is shown in Fig.4. The plotting of intrinsic capacitances C_{GS} and C_{GD} curves are done through AC small signal analysis after post-processing operation of DC solution. The capacitances between each pair of electrode are calculated by single AC frequency (1GHz) solution during a DC ramp voltage from 0V to 2.5V with a step of 0.1V. For the inversion/deep depletion region, the DIRECT parameter is added for more robust solution.



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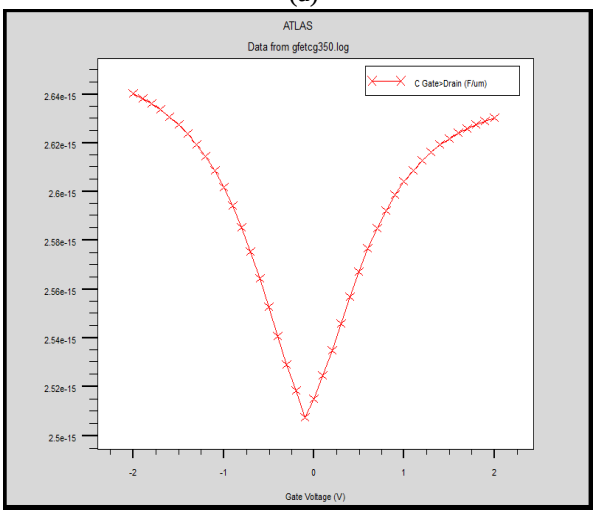
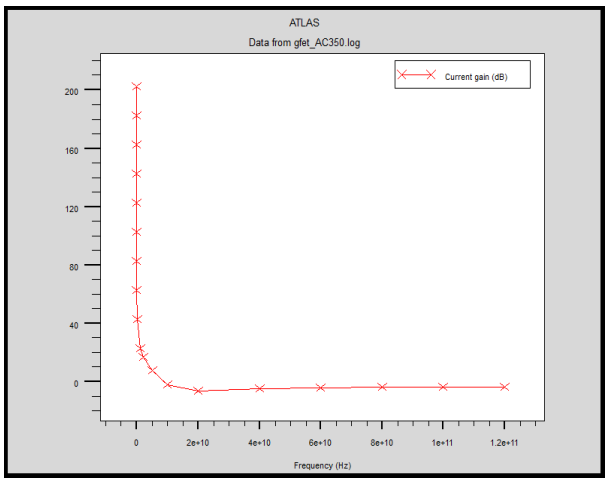


(b)

Figure: 4 Capacitance Curves (a) C_{GS} (b) C_{GD}



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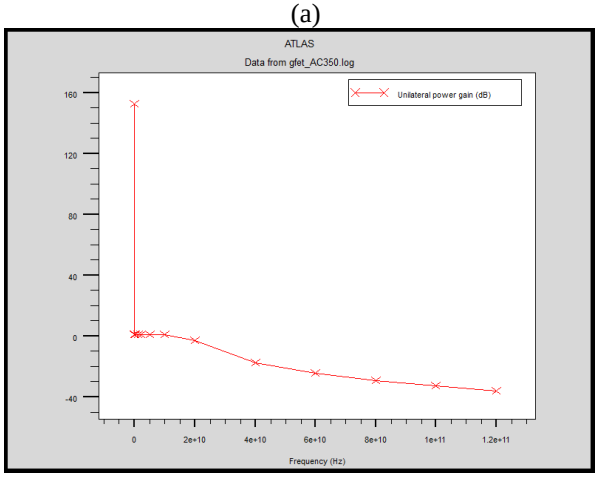

(b)

Figure5 Curves to extract f_T and f_{MAX} (a) Current gain curve (b) Unilateral power Gain curve

The cut-off frequency is the frequency at which the current drops to unity, the frequency at current gain equals 0dB. And the maximum cut off frequency is the frequency at which the power gain is unity [11]. So, in order to extract the particular values of f_T and f_{MAX}, we need to plot the current gain and unilateral power gain as a function of frequency as shown in fig 5. The above mentioned parameters in terms of the small signal parameters are defined as below in table 3. The parameters are defined considering the small signal equivalent of GFET [14] and in terms of Y-parameters and Z-parameters.

TABLE 3.PERFORMANCE PARAMETER DEFINITIONS IN TERMS OF Y AND Z PARAMETERS [8]

Parameters	***Equations***
Gate-drain cap.	$C_{GD} = -\frac{\mathrm{Im}(Y_{12})}{\omega}$

Gate-source cap.	$C_{GS} = \frac{\mathrm{Im}(Y_{11}) + \mathrm{Im}(Y_{12})}{\omega}$
Transconductance	$g_m = \mathrm{Re}(Y_{21})\lvert\omega^2 = 0$
Current gain	$h_{21} = \frac{Z_{21}}{Z_{22}}$
Cut off frequency	$\lvert h_{21}(\omega)\rvert = 1$

Extracted parameters or values of cut-off frequency and maximum frequency of oscillation are listed in table 4. Here in the table 3, *Im* and *Re* is the imaginary and real part of the respective terms. Y_{12}, Y_{21}, Z_{21}, Z_{22} are matrix elements of the y-matrix and z-matrix of the small signal equivalent circuit [14].

TABLE 4: zEXTRACTED VALUES OF FOMS OF RF TRANSISTOR

Parameters	f_T(GHz)	f_{MAX}(GHz)	*Stern stability factor(S)(GHz)*
Value	8.81	12.41	40

4. CONCLUSION

Engineering and a novel approach to simulate the RF of GFET based on a classical 2D device simulator is presented. The design and RF performance analysis of GFET is performed using TCAD simulation and the characteristics are studied. The performance parameters are obtained through ac analysis. The cut-off frequency and the maximum oscillation frequency obtained estimate the high frequency performance of GFET. It is suggested that the TCAD simulation might have the possibility to use to model the material graphene and thus the device GFET for analysis thus saving time and cost of the actual production.

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