Time Performance Improvement in DPLLs for Wireless Communication

-A Literature Survey

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Abstract:*Rapid growth in communication technology has been seen over the past few years. Current 3G and 4G systems provide enhanced features captivating more and more users. However, with the ever increasing user demand, providing satisfactory data rate or speed remains an issue. Futuristic 5G systems with hundred times faster data rates are thus already in the reckoning. Communication systems that can serve low error rates at minimum delay are the need of the hour. DPLL based receiver packages find place in modern day communication setups. In recent times, many such standalone receiver designs based on popular techniques such as Zero Crossing (ZC), polynomial fitting etc. have been proposed to exhibit satisfactory error performance. But DPLL loop action leads to degraded time performance and so current research focuses on minimizing this time delay. A detailed survey on different time performance improvement techniques for DPLL systems is presented here.*

Keywords:time efficiency, acquisition, time jitter, delay

1. Introduction

Sampled domain version of traditional phase locked loops with a digital Phase-Frequency Detector (PFD) are termed as Digital Phase Locked Loops (DPLLs) [1][2]. DPLLs play a versatile role in modern day communication setups performing carrier regeneration in non-coherent systems where the channel information is not known to the receiver [2], symbol retrieval in coherent setups for known channel [3], multiple clock distribution into sub-systems using divider units besides providing time synchronization in communication systems [2]. DPLLs are thus widely utilized in the field of communication.

Contemporary DPLL systems proposed in [1][4] stress on time efficient recovery of symbols under critically degraded channel conditions. A Zero Crossing Digital Phase Locked Loop (ZC-DPLL) with a linear PFD response, fast locking, low phase error and wider lock-in range has been proposed in [1]. Another ZC-DPLL design is suggested in [4] that introduces a hyperbolic non-linearity and a sigma-delta unit to ensure better adaption of the loop filter achieving improved time jitter and lock-in range performance under high Doppler environments. On the contrary, another class of DPLL aims to achieve significantly lower BER levels involving computationally complex processes resulting in degraded time performance. The LSPF-DPLL system in [2] and the ZC-DPLL system in [3] incorporate complex Left/Right (L/R) shift algorithms to build the Numerically Controlled Oscillator (NCO) and Digitally Controlled Oscillator (DCO) units respectively and are bottlenecked by poor time performance. Current research therefore focuses on enhancing the time efficiency of such low BER systems as in [2][3][5] and also on proposing new DPLL designs which provide an optimum balance between error and time performance. A survey on different time performance improvement techniques that have been reported for DPLL based communication systems is presented here.

The organization of the remaining portion of this paper into different sections is as follows. In Section II, the significant background details that should be kept under consideration are briefly discussed. Section III emphasizes on evolution of DPLLs in relation with different generations of communication technology. The current state of research in DPLL technology is also identified in this section. In Section IV, a detailed survey and analysis of different time performance improvement techniques suggested for DPLLs is presented. Finally, Section V summarizes the discussion.

2.Background Considerations

DPLLs provide a generic communication system design providing acceptable performance levels for widely varying wireless environment [1][6]. Also, DPLL principle being phase-based provides generic transmission model with phase containing the most crucial information of any signal [2][5]. However, for utilizing DPLL efficiency, choosing a proper transmission scheme is inevitable. Also, a detailed analysis of different wireless channel environments that DPLL based setups may be subjected to is crucial. A theoretical analysis of different sub-systems of the DPLL is needed for proper understanding of loop action.

2.1 QPSK Signal Model

Quadri-phase signals conserve bandwidth significantly through dibit transmission maintaining well separated decision boundaries for low BER as suggested in [2][6][7]. DPLL systems provide optimum performance with QPSK signals as suggested in [2][5][8] and thus are popularly used as standard modulation schemes for DPLL based

communication [3]. The quadrature phase signals are defined as shown in eq. (1)

$$s(t) = A\cos(2\pi f_c t + \theta_i) \qquad (1)$$
$$0 \le t \le T, i = 1,2,3,4$$
$$\theta_i = \frac{(2i-1)\pi}{4}$$

where, A is the symbol amplitude, f_c is the frequency for transmission and θ_i is the QPSK phase. The four possible phases are: $\frac{\pi}{4}, \frac{3\pi}{4}, \frac{5\pi}{4}, \frac{7\pi}{4}$.

2.2 Wireless Faded Environment

Fading channel models with Rayleigh and Rician probability distributions provide statistical estimates of realistic wireless environment for urban and rural areas respectively as discussed in [2][5][7] and thus DPLL based communication systems are tested under them.

The received signal *s(t)* under Rayleigh faded wireless channel for NLOS condition between transmitter and receiver is given by eq. (2):

$$s(t) = \sum_{k=1}^{N} a_k \cos(\omega_c t + \omega_{dk} + \emptyset_k) \qquad (2)$$

where a_k is the k^{th}path gain, ω_c is the carrier frequency in radians, ω_{dk} is angular Doppler frequency due to relative transmitter-receiver relative motion for k^{th}path and ϕ_k is the random phase for the k^{th}path[2][5][9]. The probability density function for Rayleigh Distribution is shown in eq. (3):

$$F(r) = \frac{r}{\sigma^2}\exp\left(-\frac{r^2}{2\sigma^2}\right) \qquad r \ge 0 \qquad (3)$$

Similarly, the received signal *r(t)* for Rician Faded wireless channel where there exists a strong LOS component along with the NLOS scenario is given by eq. (4):

$$r(t) = s(t) + k_d\cos(\omega_c t + \omega_d t) \qquad (4)$$

where *s(t)* is the contribution due to the NLOS components, k_d indicates the signal strength for the LOS component, and ω_d is the angular Doppler frequency component in radians [2][5][10]. The probability density function for Rician distribution is expressed by eq. (5):

$$F(r) = \frac{r}{\sigma^2}\exp\left(-\frac{r^2+k_d^2}{2\sigma^2}\right).I_o\left(\frac{r k_d}{\sigma^2}\right) \qquad r \ge 0 \qquad (5)$$

$I_o(.)$ represents the 0^{th} order modified Bessel Function of first kind.

DPLL based communication systems have been suggested in [2] for analysis under more accurate estimates of Nakagami-*m* fading channel which represents a generalized picture combining fading effects of Rayleigh and Rician models. The value of *m* is varied to change the density function for statistical estimate of the channel to provide realistic channel estimates.

2.3 Components of a DPLL

The components of a typical DPLL are shown in Figure 1.

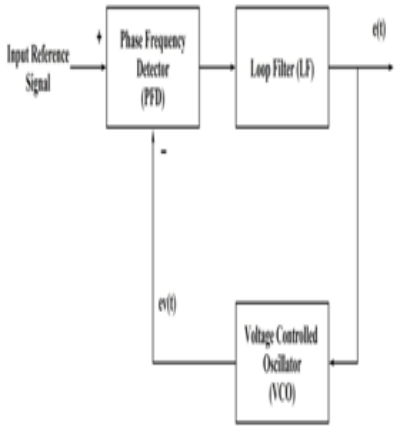

Figure 1: Components of Digital Phase Locked Loop

A typical DPLL consists of *three* typical components which are discussed below:

2.3.1 Phase Frequency Detector (PFD)

The phase of the incoming reference signal is compared with that of the locally generated signal of the oscillator to detect the phase error between two signals. It is popularly realized as a digital multiplier which multiplies both the signals to obtain a resultant signal containing a high frequency term and another slow changing term which gives the phase difference between the two signals [2][3][11][12]. The action of the PFD has been illustrated in eq. (6), (7) and (8).

Let *x(n)* be the input signal such that

$$x(n) = sin(\omega n + \theta_i) \qquad (6)$$

where ω and $\theta_i$are the angular transmission frequency and phase of the reference signal respectively. The feedback element of DPLL i.e. Voltage Controlled Oscillator (VCO) will generate a sinusoidal signal $e_{VCO}(n)$ given by eq. (7)

$$e_{VCO}(n) = A\cos(\omega_{VCO} + \theta_{VCO})n \qquad (7)$$

where ω_{VCO} and θ_{VCO} are the angular frequency and phase of the VCO's generated signal. If the output of the phase detector is denoted by $v_d(n)$ then

$$v_d(n) = K\sin(\omega n + \theta_i) \times \cos(\omega_{VCO} n + \theta_{VCO})$$
$$v_d(n) = \frac{K}{2}[\sin(\omega + \omega_{VCO})n + \theta_i + \theta_{VCO} + \sin((\omega - \omega_{VCO})n + \theta_i - \theta_{VCO})]$$

where K is the phase detector gain. If $\omega = \omega_{VCO}$ then,

$$v_d(n) = \frac{K}{2}[\sin((2\omega n + \theta_{VCO}) + \theta_i) + \sin(\theta_i - \theta_{VCO})] \qquad (8)$$

Eq. (8) represents output of the PFD and it is fed to the Loop Filter.

2.3.2 Loop Filter (LF)

The PFD output contains two terms, one is a high frequency component and the other is a slow changing phase error signal which stores useful information, so the loop filter eliminates the high frequency component acting as a low pass filter and at the output of the LF, we have only the phase error signal [2][3]. Eq. (9) and (10) govern the filtering action as below:

Let $v_f(n)$denotes the filter output:

$$v_f(n) = \frac{K}{2}[sin(\theta_i - \theta_{VCO})] \quad (9)$$

If $(\theta_i - \theta_{VCO}) \ll 1$, then approximation of $v_f(n)$ is given by

$$v_f(n) = \frac{K}{2}[\theta_i - \theta_{VCO}] \quad (10)$$

Eq. (10) is the loop filter output and it is fed to the VCO.

2.3.3 Voltage Control Oscillator (VCO)

It represents an oscillator which adjusts the local oscillator's free running frequency in accordance with the control input, i.e. the LF output [3]. The control voltage as depicted in eq. (10) is fed to the VCO which varies the frequency of the local oscillator to achieve the 'phase-frequency locking' of both the signals [5][11]. In DPLLs a sampled version of the VCO is used which is represented by eq. (11) as below:

$$f_{VCO} = (\frac{M}{2^j} + c) \times f_{free\ running} \quad (11)$$

where f_{VCO} is the adjustable VCO frequency, M is an integer value lying in the range $-2^{j-1} \leq M \leq 2^{j-1}$, c is a constant value, j is number of bits for digitization and $f_{free\ running}$ is the free running VCO frequency.

3.DPLL Technology over the years

Communication technologies have evolved over the years and indeed very rapidly in the recent times. DPLLs have always been popular in different aspects of communication technology mainly because of its versatility and generic nature [2]. DPLL technology has therefore evolved hand in hand with the evolution of different generations of communication technologies and to understand this parallel evolution, a brief discussion on evolution of different generations of communication technologies and the simultaneous evolution of DPLLs is presented here. Also, this discussion ultimately helps in tracking the current state of research in DPLL technology.

3.1 Evolution of Communication Technologies

In the last two decades or so, communication technologies have rapidly evolved with the introduction of a number of new communication standards which exhibit a very subtle balance between crucial parameters such as error performance, power levels required for transmission and reception, bandwidth efficiency, throughput etc. and also on-chip circuitry optimized in terms of device level power and speed of operation. After an initial advent of the 1st Generation Communication standards popularly known as 1G standard in USA in 1940s (and Europe in 1950s), mobile communications gained popularity with Cordless Telephones (CTO and CTI), paging systems, private mobile radio systems, cellular systems such as AMPS etc. and also mobile satellite systems such as INMARSAT [13]. However, mobile communications were still not very popular among the masses and were mainly used by the defence organisations and powerful bodies mainly because of the high setup and usage costs. The 2G standards came up with the introduction to GSM (Global System for Mobile Communications) in 1990s in Europe. Unlike 1G which was limited to voice, 2G provided both voice and limited data services using digital modulation schemes to popularize mobile communications [2][13]. The mobile technology using General Packet Radio Services (GPRS) were termed as 2.5G systems enhancing the data capacity of GSMs. Packet Switched techniques replaced Circuit Switched techniques for higher link efficiency. Rapid growth was experienced from the stage when 2.5G standards were introduced. The 3G technology aims at providing a single standard network instead of different networks in USA, Europe etc. to ensure reusability of communication devices and specifications. 3G adds multimedia services, live video streaming, audio and graphics applications to the second generation mobiles [13]. From the period when 3G wasn't even fully implemented, limited speed (maximum of 2 *Mbps*) was a big issue and so it led to the need for 4th Generation Mobile Communications (4G). It aims at achieving data transfer speeds up to 50 times that of 3G networks with Long Term Evolution (LTE) as a base. With huge rise in user demand, low latency 5G technology is being already talked about and it aims at meeting the end user requirements with 100 times higher data rate per user and 1000 times more capacity [13].

3.2 Evolution of DPLLs for Communication

Digital Phase Locked Loops play a very significant role in the evolution of contemporary communication systems. Communication technologies have evolved in a massive manner with prime focus on optimum reception of signals. Till around the period of 1930s, Armstrong's Super Heterodyne receiver which performed signal reception by a number of frequency range translations of the received signal was widely used in spite of the complex circuitry involved. However, there was a continuous effort on the part of scientists of that time to develop an alternative to the complex design. In 1932, the first automatic synchronization device termed as the 'homodyne' or 'direct conversion receiver' was developed [2][5] to directly tune to a single locally generated frequency. This aspect was presented in 1932 by Henri de Bellescize, in the French journal L'Onde Lectrique and thus popularized the Homodyne as the modern day Phase Locked Loops [2]. The on-chip implementation of PLLs on monolithic ICs was introduced by Signetics in 1969 followed by RCA introducing the CD4046 CMOS Micro power PLLs a few years later establishing Phase Locked Loops as an efficient communication device[2][3].

3.3 Current State of DPLL based Communication

The current research trends in the field of DPLL based Wireless Communications doesn't just concentrate on the traditional aspect of error rate minimization. It also equally emphasizes on device level implementation of the standard communication systems that are designed to suit particular error rates. It has been recently emphasized on achieving good DPLL performance in terms of reduced supply power levels, enhanced speed, enhanced throughput, reduced delay, improved time efficiency and reduced time jitter[13]. Efficient communication is a time dependant process and delays of any form degrade the performance of the system by a large extent [12]. A contemporary aspect of research is to enhance time performance of DPLL systems by reducing delays in terms of time jitter, linearization of processes, processing time etc.

4. Time Performance Improvement in DPLL Systems

DPLL systems suffer from degraded time performance due to many reasons which include jitter delay due to internal noise circulation, constantly high system bandwidth, non-linear PFD response leading to high locking time, redundancies in design of DPLL sub-units and intensive computations leading to processing delays etc. [1][2][3][10]. Some effective techniques to improve time efficiency are outlined below:

- linearization of PFD response to reduce lock time.
- two-step acquisition: frequency and phase track with high and low system bandwidth respectively.
- simplifying the feedback path to achieve fast lock.
- reducing redundancies in DPLL sub-units for faster loop action.
- a possible way could also be parallel execution of intensive computations on multiple processor cores.

To have a clear idea of the different techniques used for time efficiency improvement, a detailed survey is carried out below.

The design and implementation of a Bang-Bang Digital PLL was discussed in [14]. The proposed model presents a fast locking Bang-Bang Digital LC PLL design which uses multiphase output using a magnetically-coupled loop of oscillators operating at 25 *GHz*. The proposed design uses a novel oscillator design to generate eight output phases using magnetic coupling. A passive network interconnects the four DCOs to generate eight different phases at the cumulated output [15]. This structure leads to an interconnect between the oscillators and leads to a standard area improvement of *2x* times. This leads to minimization in terms of power and makes it a suitable candidate of low power wireline communications. Fast wake up of the PLL system is achieved by calibrating the phase with respect to the input reference signal using a first order loop leading to fast phase locking of the system as stated in [12] and also in [15]. The proposed model is implemented on a 40 *nm* CMOS technology and exhibits low lock time, minimum jitter and considerable power saving as stated in [12][15].

An All Digital PLL which has been used for frequency synthesis in RF wireless applications is presented in [16]. To avoid analog tuning which requires fine resolution, DCO is used instead of VCO. In [16], charge pumps are replaced by a time to digital converter and first order simple digital loop filter which are build around digital circuitry which ease the implementation as mentioned in [2] and utilize the sophisticated digital circuitry. The proposed model presents novel techniques to achieve ultra-fast frequency acquisition in as less as 50 μs as stated in [16] in parallel to maintaining low levels of the phase noise and also spurs internally within the system during the transmission and reception. This is made possible by varying the loop bandwidth as discussed in [16].

A DPLL design based on the Bang-Bang Algorithm is proposed in [12] and typically consists of a Bang-Bang PFD, a finite state machine (FSM), a digital loop filter (DLF), a Digitally Controlled Oscillator (DCO) with Delta-Sigma Modulator (DSM) and a divider chain for the desired tuning frequency. The components and functions of a Bang-Bang DPLL have already been discussed in [4][11][12][14] and some other related works. The Bang-Bang Algorithm however has been modified in [12] by adding a Lock Monitor unit (LM) which selects in between the conventional Bang-Bang algorithm and the modified one under conditions of phase error. The system settles down at around 300μs when the modified algorithm is applied in [12] as compared to poor 1.06 *ms* for the old design. The proposed ADPLL is implemented on 90 *nm* CMOS process [12][17] and exhibits low jitter of 2.622 *ps* and is a good option for fast communication.

A novel parallel processing architecture for digital carrier recovery (CR) which is suitable for ultra high speed coherent optical receivers (more than 100 *Gbps*) is presented in [18]. The feedback or non-linear path leads to additional time in settling down of the loop response ultimately slowing down the system's time performance [18][19].The proposed model incorporates parallel processing in the feedback loop of traditional DPLLs as stated in [18]. This leads to a low latency parallel DPLL architecture which computes the feedback loop operations in approximately lesser number of reference clock cycles than the serial DPLL thus leading to speed up of the DPLL performance maintaining capture range and bandwidth making it suitable for implementing in both ASIC and FPGA platforms. The system is tested under QPSK with parallelism equal to 16 at 10 *Giga-symbols per second* and exhibit much precise values of $k_p$and k_i while having a capture range of 1 *GHz* which is the maximum theoretical frequency offset thus proving the superiority of PDPLL design in [18].

A novel model for an All Digital Phase Locked Loop that has been proposed for providing higher performances for wideband frequency tracking and also at the same time provides noise reduction while shortening the time required for settling down to the synchronized state where the input reference signal and the DCO's signal are in lock as stated in [20]. It shows good performance in terms of fast acquisition and also noise reduction which is achieved by incorporating a 'controllable shift filter' which cuts down the system noise to the minimum. Such aspects of the shiftable filter which adapts to a reference frequency to nullify noise have been discussed in [3] also. It provides wideband frequency tracking with aid from the module incorporated for synchronizing to the desired frequency as discussed in [20]. The proposed design can be packed as an IP core for SoC applications.

A Flash Fast Locking DPLL system using 0.18 μm CMOS process and a supply of 3.3 *volts* power supply is proposed in [21]. Similar work has been discussed in [22]. The design proposed in [21] operates in two stages: firstly, the coarse tuning stage where the desired frequency is tuned to lock the DPLL to exactly that frequency. The coarse tuning setup uses a Flash A/D converter instead of the Successive Approximation Converter presented in [22]. The second stage of operation is the fine tuning or tracking of the signal in its proper phase which is common to all DPLL structures. The proposed system in [21] shows better time performance as compared existing DPLL designs and for sufficient number of frequency comparators, the lock time will always be lower than 140 *ns* as compared to traditional DPLLs which have lock time up to 290 *ns* [21][22].

Some notable time performance improvement techniques proposed for DPLLs in recent times have been outlined in Table I in terms of technique used, performance parameters and results obtained.

TABLE 1: VARIOUS TIME PERFORMANCE IMPROVEMENT TECHIQUES FOR DPLLS

S.No	Technique Used	Performance Parameter and Result
1.	Digital LC-PLL design proposed in [14]. Phase is calibrated in terms of input reference; LC unit leads to magnetic coupling reducing latency.	Locking Time achieved is 100 *ns*. Phase Error is less than 2º.
2.	ADPLL instead of DPLL in [16]; time to digital converter instead of charge pump; first order loop.	Acquisition Time as low as 50 μs.
3.	Modified version of Bang-Bang (BB) Algorithm in [12]; Lock Monitor Unit checks phase error crossing reference.	Locking Time is 300 μs as compared to BB-locking at 1.06 *ms*; low jitter of 2.622 *ps*.
4.	Parallel Processing Architecture for feedback loop is proposed in [18] for DPLL carrier recovery unit; QPSK symbols are processed.	Lesser number of reference clock cycles; provides similar BER performance as serial DPLL with parallelism of 16 at 20 *Gbps*.
5.	ADPLL proposed in [20] for wideband frequency tracking; controllable shift filter to cut down system noise; uses two step-acquisition.	Lesser number of reference clock cycles; returns to stable state in as low as 4 *clock cycles*.
6.	A Flash based DPLL is proposed in [21]; uses two-step acquisition, coarse tune stage consists of a Flash A/D converter; fine tune phase tracking is common for all DPLLs.	Low lock time of 140 *ns* Compared to traditional designs that need time upto 290 *ns*.
7.	A SAR based DPLL is proposed in [22]; two step acquisition with coarse tune stage realized by a Successive Approximation based A/D converter.	Percentage saving of lock time as compared to contemporary designs is around 50 *percent*.
8.	ZC-DPLL proposed in [4] for high Doppler Environment; hyperbolic non-linearity and Σ-Δ modulator block.	Improvement in time jitter delay by a factor of 6.4 to previous design.
9.	No delay TDL proposed in [11]; phase shifter instead of delay unit.	Phase plot shows faster locking; lock-in range improvement by 3.68.
10.	ZC-DPLL Frequency Synthesizer in [6]	Fast lock on phase plot

Based on the tabulated information in Table I and the detailed discussion carried out in this section, it can be stated that time performance improvement for DPLLs is currently a focused area of research because DPLLs are widely deployed in communication systems and time efficiency is a key concern. It can be seen from the study that most designs that have been proposed focus on time performance improvement from the point of view of parallelized architecture [23], reducing the jitter tracking delay [24], linearizing the PFD response [25], reducing the feedback delay [26] etc. But there remains huge scope for DPLL time performance improvement from the aspect of reducing processing time.

5. Conclusion

DPLL technology has evolved over the years and plays a crucial role in modern day communication systems due to its versatile nature. The performance of communication systems is bottlenecked by time delay. Systems which can optimize well between time and error performance are preferred. DPLL is composed of a number of sub-units including a feedback loop and are limited by delays. So, time efficient DPLL systems have been focused in recent times. A survey on different time performance improvement techniques proposed for DPLLs is presented here. From the detailed survey, it can be concluded that time performance of DPLLs is an important issue and needs to be addressed properly. Most recent designs focus on improving time efficiency from the aspect of reducing delays arising due to jitter, non-linearity of PFDs etc. However, emphasis should also be laid upon reducing processing delays in DPLL systems.

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