A Novel Fault Tolerant Full Bridge DC/DC Converter for Photovoltaic application

Shamkumar B. Chavan [1], Mahesh S. Chavan[2]
[1]Department of Technology, Shivaji University, Kolhapur, Maharashtra India
sbc_tech@unishivaji.ac.in
[2]Department of Electronics Engineering, KIT College of Engineering, Kolhapur, India.
maheshpiyu@gmail.com

***Abstract:** Power switches in converters are prone to open and short circuit faults. Faulty power switch in converters worsens the converter performance and it may result in failure of other devices also. Further when main power switch fails, it results in breakdown of entire system. Therefore for reliability improvement of full bridge DC/DC converter in PV system, this research paper presents a novel fault tolerant converter topology for exact faulty power switch localization and isolation from main path so that redundant faulty power switch can be brought in action and still system will provide desired output power. The converter presented here need two redundant power switches and relays to provide fault tolerant competence. It has four operating states which are normal state, faulty state, fault diagnostic state and fault recovery state. In the technique presented here RMS current at given test points is computed and compared with threshold RMS current for determination of faulty power switch. Graph theory is used to show the topological equivalence of converter in normal and fault recovery states. Simulation and experimental results have shown that converter efficiency remains same in both normal and fault recovery state.*

***Keywords:** Fault tolerant full bridge converter for PV application, Converter fault detection, Relay operated fault tolerant converter, redundancy based fault tolerant converter*

(Article history: Received: 22nd July 2020 and accepted 26th December 2020)

I. INTRODUCTION

Surveys and literatures have shown that power switches in converters are failure prone components suffering to OC and SC failures [1], [2], [4], [19], [20]. Therefore importance of reliable converter designs is discussed [21]-[24]. Researchers have proposed power switch fault diagnosing techniques and fault tolerant architectures for DC-DC converters. Localization and isolation of exact faulty component and initiating the fault tolerant action are important issues in converter reliability improvement. In remotely located PV stations, faults in converters could result in lowered power generation, malfunction etc. Manual fault diagnosis and repairing is time consuming. Hence implementation of fault diagnosis and tolerant scheme for converter will improve the system reliability. Recently redundancy based converter architectures are proposed which automatically localizes exact faulty power switch and brings converter in recovery state [5]-[7], [9]-[14], [16]-[18]. Giovanni et al [1] reports that power processing circuits must have high reliability, efficiency and modularity. Inverters, controllers, system components, interconnects, batteries etc. are failure prone, environmental conditions affect the performance of these components and of PV modules [1],[2] hence reliability of power processing circuits is an important issue. Hugo et al informs that the [3] life span of PV array is more than that of power processing circuits. A survey [4] on reliability of power electronic converters reported that power switches are the most failure prone components due to several reasons, capacitors, resistors, inductors, gate drivers; connectors are also found failure prone. Considering failure prone nature of power electronic converters it is necessary to focus on reliability improvement aspects at design stage. Many researchers have valuable contribution in development of OC power switch fault tolerant schemes for converters. Eunice et al [5] has presented an open circuit fault tolerant three level boost converter for photovoltaic application using additional devices like triac, inductor, capacitor and PV panel. Pei et al presented power switch OC [6] and SC [14] fault diagnosis and tolerant scheme in an isolated phase shifted full bridge DC-DC converter. In [7] open circuit fault diagnosis scheme for power switch and diode in dual active bridge DC-DC converter has been presented. Wu et al [8] states that fault tolerant schemes with reduced cost and complexity are important. Khalid et al presented OC and SC fault tolerant scheme for H bridge converter which works in multiple modes [9]. Redundant transistor based fault tolerant scheme is presented [10][11] for step down DC-DC converter. Cascaded step up and step down fault tolerant converter for PV system is designed [12]. Fault tolerant scheme for boost converter in PV application is presented [13] which monitors inductor current for one cycle. Reference [15] deals with detection of power switch fault in PWM converters. Fast OC and SC faulty power switch diagnosis scheme without any additional voltage sensor is presented [16] in which redundant switches are used for fault recovery. OC power switch fault diagnosis scheme in interleaved DC-DC converter based on measurement of DC link current is presented [17]. Fault tolerant resonant full bridge DC-DC converter is presented [18], in which converter is operated in half bridge mode on arrival on power switch fault, further use of doubler stage at rectifier is suggested. Module level redundancy is proposed in converter where input modules are paralleled while output is in series to achieve fault tolerance, here master slave strategy is used [25]. Two FBDCDC converters are paralleled and controlled to achieve fault tolerant operation [26], this requires additional converter module. In [27] architecture is proposed in which input is in series while outputs are paralleled.

Considering the reliability issues in converters, this paper presents an open switch fault tolerant full bridge DC/DC converter topology in which mechanism for localizing exact faulty power switch and to initiate fault tolerant action is proposed, the scheme presented here is applicable for open power switch faults. It is based on redundancy approach and only few numbers of components are required to add, it is cheaper and in recovery state output power remains same like in normal state. The presented converter is designed and tested for PV application. IGBTs are used as switching devices.

II. PROPOSED FAULT TOLERANT CONVERTER TOPOLOGY AND CONTROL SYSTEM

The proposed open power switch fault diagnostic and tolerant full bridge DC/DC converter topology applicable to photovoltaic system is shown in fig. 1. In this topology, branch 3 having redundant power switches Q5, Q6 and relays 1 and 2 are added to provide fault tolerant competence. In normal working state branches 1 and 2 are connected to NC terminal of relay 1 and 2 while branch 3 is connected to NO terminal of relays. Due to this, branches 1 and 2 remain active in normal working states. In normal i.e. fault free condition, power switches Q1-Q4 and Q3-Q2 conduct in pair. The RMS current at test points TP1 and TP2 is computed using the expression $I_{rms} = I_{pv}.\sqrt{\text{Duty Cycle}}$. The converter has four states viz. i) normal state – In this state the converter work without any fault, the power switches Q1 to Q4 remain active and desired output power is obtained. Fault precursors are regularly monitored at test points TP1 and TP2. ii) Faulty state- In this state abnormal fault signatures are observed at TP1 and TP2 which is indication of any power switch open circuit fault. iii) Fault diagnostic state- In this state the exact faulty power switch is localized by using the novel scheme proposed in table 1 and in flowchart in fig.3. iv) Fault recovery state- In this state the branch with faulty power switch is isolated by using relays and third redundant branch is brought in action, such that desired output power is obtained.

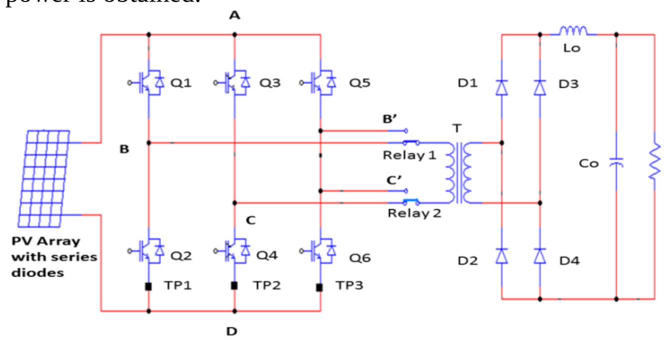


Fig. 1. Proposed novel fault tolerant DC/DC converter for PV application

Table 1- Fault diagnosing signatures and tolerant mechanisms

TP1$	TP2$	TP1_FD#	TP2_FD#	Faulty power switch	Operating switches		Relay 1	Relay 2
					First cycle	Second cycle		
Normal working state (No fault)								
H	H	----	----	None	Q1,Q4	Q3,Q2	NC	NC
Faulty states								
H	L	L	H	Q1	Q5,Q4	Q3,Q6	NO	NC
L	H	L	H	Q2	Q5,Q4	Q3,Q6	NO	NC
L	H	H	L	Q3	Q1,Q6	Q5,Q2	NC	NO
H	L	H	L	Q4	Q1,Q6	Q5,Q2	NC	NO
L	L	L	H	Q1,Q2	Q5,Q4	Q3,Q6	NO	NC
L	L	H	L	Q3,Q4	Q1,Q6	Q5,Q2	NC	NO

H- RMS current at test points TP1 and TP2 is above threshold level
L – RMS current at test points TP1 and TP2 is below threshold level
$TP1 - TP1 RMS current (Q3-Q2) pair in operation (Normal state)
$TP2 - TP2 RMS current (Q1-Q4) pair in operation (Normal state)
#TP1_FD- TP1 RMS current, fault diagnosing state- Relays to NO position & (Q1-Q2) pair in conduction
#TP2_FD- TP2 RMS current, fault diagnosing state- Relays to NO position & (Q3-Q4) pair in conduction

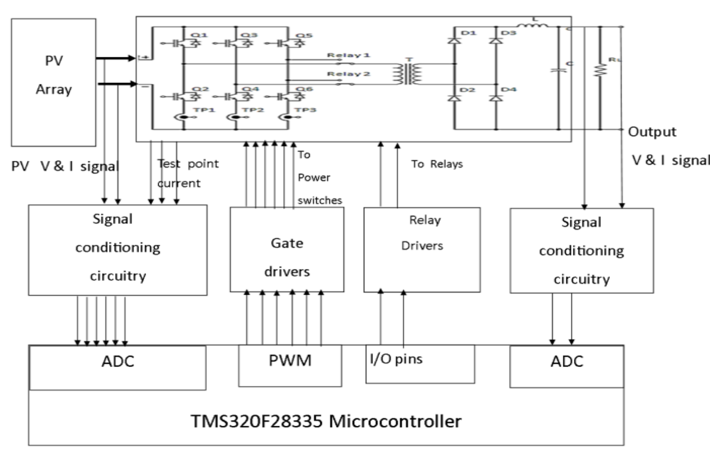
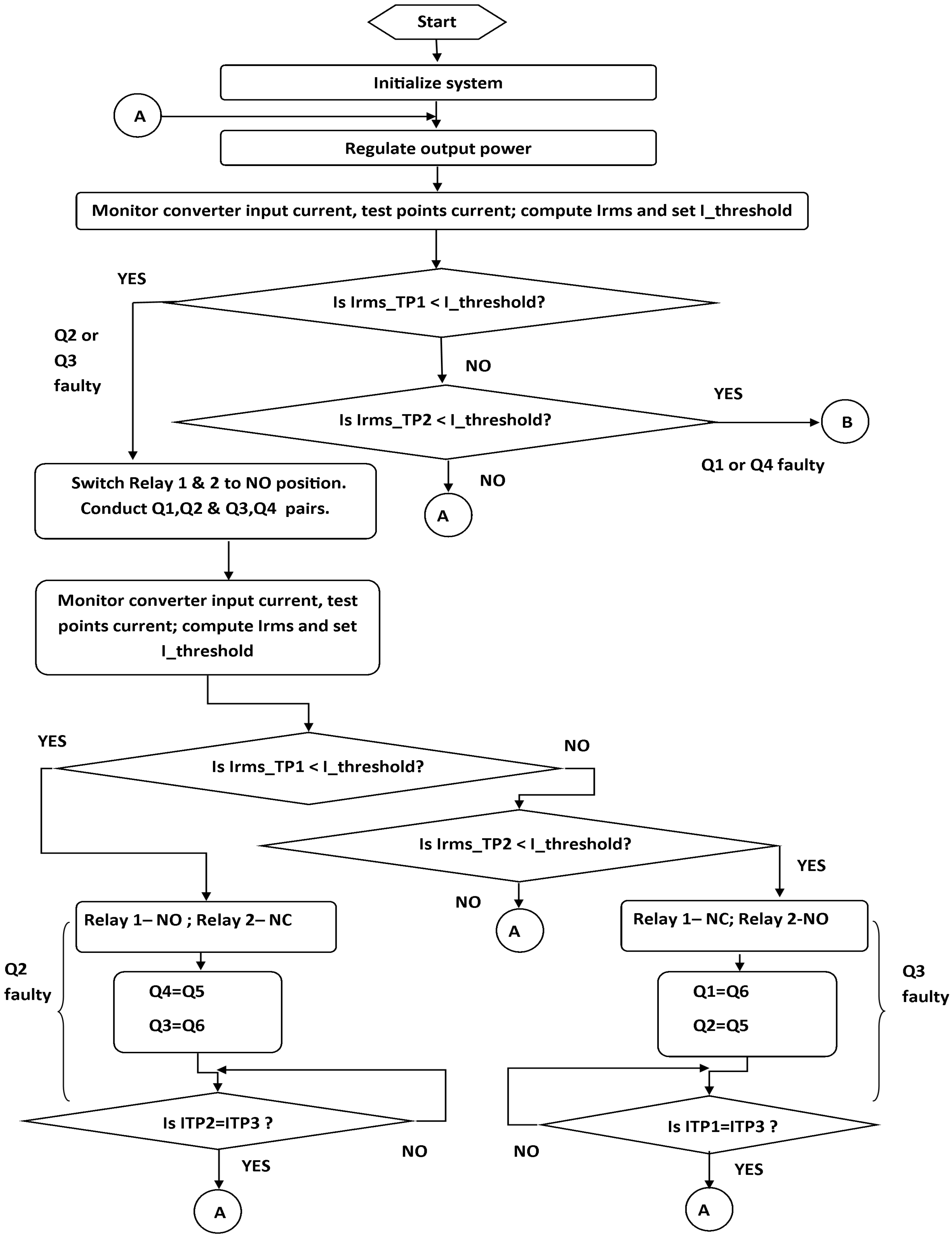


Fig.2. System block diagram

PV modules / array have series diodes.

III. FAULTY POWER SWITCHES LOCALIZATION AND FAULT RECOVERY ALGORITHM



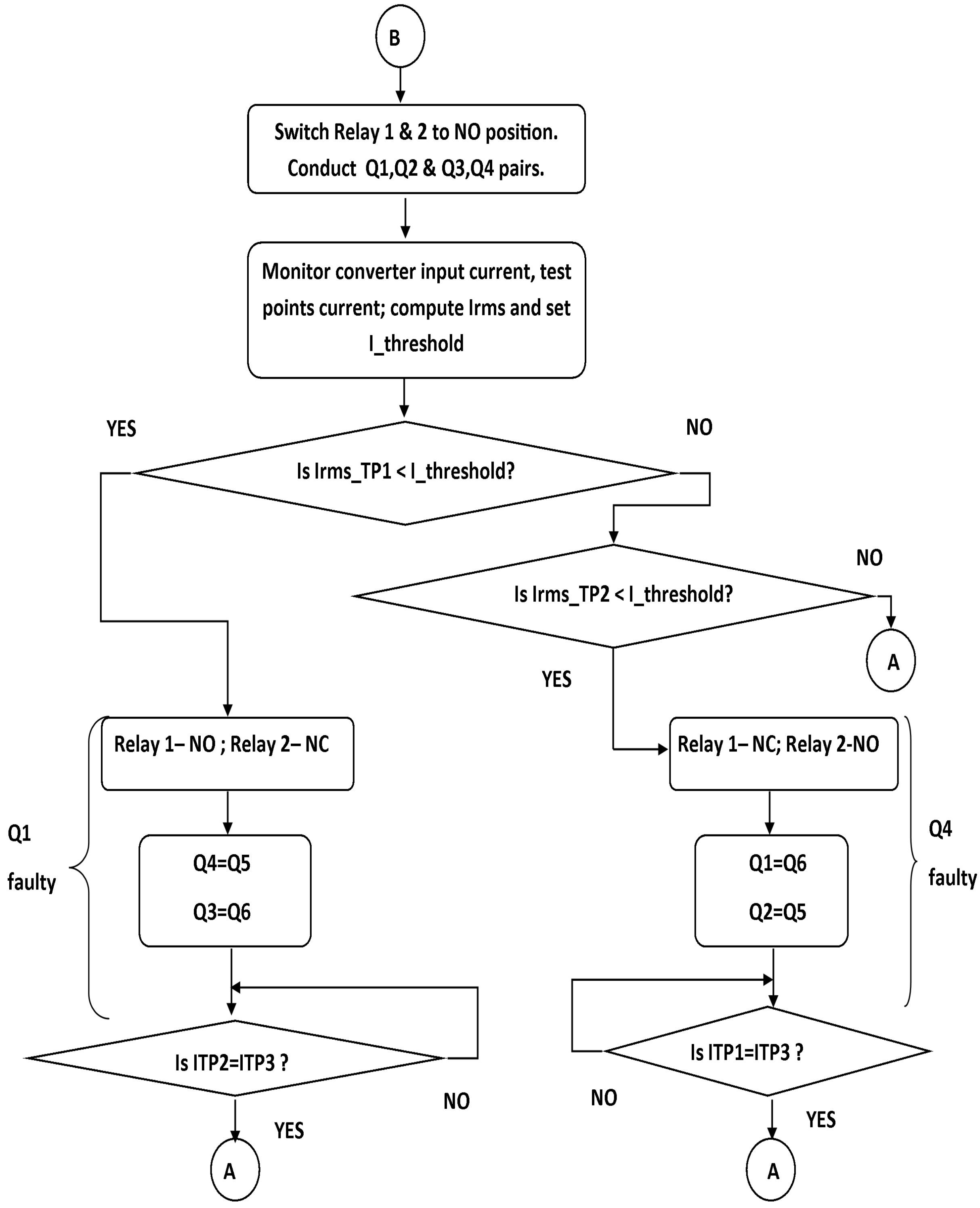


Fig. 3. a), b) System flow chart

I_{RMS}_TP1 – I_{RMS} at test point TP1
I_{RMS}_TP2 – I_{RMS} at test point TP2

Fig. 2 shows the system block diagram. The controller regulates output power and monitors current at PV array, at output and at test points TP1-TP2. For diagnosing fault it regularly computes I_{RMS} current at test points and compares it with threshold value. Flow charts in figures 3a, 3b describes operation in more detail.

Case 1. I_{RMS} at TP1 below threshold current

This is indication of open switch fault in power switch Q2 or Q3. To localize exact faulty power switch relays 1 and 2 are switched to NO position, this isolates power switch H-bridge from transformer primary. Power switches Q1 to Q4 in bridge are operated with same frequency and phase so that current passes through both branches and can be monitored at TP1 and TP2. In this state RMS current below threshold level at TP1 indicates open switch fault in transistor Q2 while current below threshold at TP2 indicates open switch fault in Q3. For Q2 open fault, the controller maintains relay 1 at NO and relay 2 is switched to NC. Due to action of relay 1 branch 1 is isolated and fault tolerant branch3 get connected to transformer primary. Controller switches OFF transistors Q1-Q2 and transistors Q3, Q4, Q5 and Q6 are operated. In fault recovery state Q3-Q6 and Q4-Q5 pairs are diagonally operated. For Q3 open switch fault , the controller positions relay 2 at NO and relay 1 is switched to NC. Action of relay 2 isolates branch 2 and brings fault tolerant branch 3 in operation. Controller switches OFF Q3 and Q4 and transistors Q1, Q2, Q5, Q6 are operated. In fault recovery state Q1-Q6 and Q2-Q5 pairs are diagonally operated.

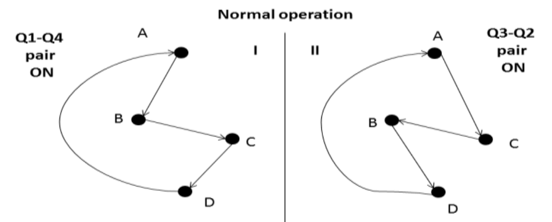
Case 2. I_{RMS} at TP2 below threshold current

RMS current at TP2 below threshold level indicates open switch fault in transistor Q1 or Q4. To locate exact faulty switch controller switches both relays to NO position. All power switches are operated with same frequency and phase. In this state current at test points is monitored, RMS current below threshold level at test point TP1 indicates Q1 as OC faulty, hence to isolate branch 1 and to bring fault tolerant branch 3 into action relay 1 remains at NO position while relay 2 is switched to NC position. In recovery state Q3-Q6 and Q4-Q5 transistors are operated. RMS current at test point TP2 below threshold level indicates that power switch Q4 is open switch faulty, hence controller keeps relay 2 at NO so that branch 2 is isolated and fault tolerant branch 3 is brought into action. In recovery state transistors Q1-Q6 and Q2-Q5 are diagonally operated. In all cases unused power switches are switched OFF. Flow charts in figure 2 and table 1 describe the converter operation.

IV. RESULTS AND DISCUSSION

A. Topological equivalence in fault recovery states using graph theory approach

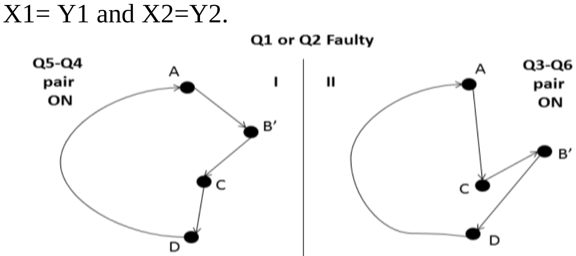
Graph theory is used to show the topological equivalence in normal and fault recovery configurations. The nodes A, B, C, D, B' and C' are shown in figure 1. Transformer secondary side along with diodes and filter are not shown in graphs because they work like in normal converter and don't have role in proposed fault tolerance scheme. During fault free operation, the graphs in cycle 1 and cycle 2 are shown and their matrices are represented by X1 and X2 in fig. 4.



$$X1 = \begin{array}{c|cccc} & A & B & C & D \\ \hline A & 0 & 1 & 0 & 1 \\ B & 1 & 0 & 1 & 0 \\ C & 0 & 1 & 0 & 1 \\ D & 1 & 0 & 1 & 0 \end{array} \qquad X2 = \begin{array}{c|cccc} & A & B & C & D \\ \hline A & 0 & 0 & 1 & 1 \\ B & 0 & 0 & 1 & 1 \\ C & 1 & 1 & 0 & 0 \\ D & 1 & 1 & 0 & 0 \end{array}$$

Fig.4. Description of original DC/DC converter in graphical and matrices form

When any power switch Q1 or Q2 from branch 1becomes faulty, branch 1 is discarded by relay 1 and the fault tolerant branch 3 get activated. The NO terminal of relay is indicated by node B'. Fig. 5 shows the graph when branch 1 in converter is faulty and it acts upon branch 2 and branch 3. The graphs in cycle 1 and cycle 2 are shown in fig. 5 and their equivalent matrices are given by Y1 and Y2. It can be seen that X1= Y1 and X2=Y2.



$$Y1 = \begin{array}{c|cccc} & A & B' & C & D \\ \hline A & 0 & 1 & 0 & 1 \\ B' & 1 & 0 & 1 & 0 \\ C & 0 & 1 & 0 & 1 \\ D & 1 & 0 & 1 & 0 \end{array} \qquad Y2 = \begin{array}{c|cccc} & A & B' & C & D \\ \hline A & 0 & 0 & 1 & 1 \\ B' & 0 & 0 & 1 & 1 \\ C & 1 & 1 & 0 & 0 \\ D & 1 & 1 & 0 & 0 \end{array}$$

Fig.5. Converter topology description in Q1 or Q2 fault recovery state

When any power switch Q3 or Q4 from branch 2 becomes faulty, branch 2 is discarded by relay 2 and the fault tolerant branch 3 get activated. The NO terminal of relay 2 is indicated by node C'. Fig. 6 shows the graph when branch 2 in converter is faulty and it acts upon branch 1 and branch 3. The graphs in cycle 1 and cycle 2 are shown in fig. 6 and their equivalent matrices are given by Z1 and Z2. It can be seen that X1= Y1=Z1 and X2=Y2=Z2.

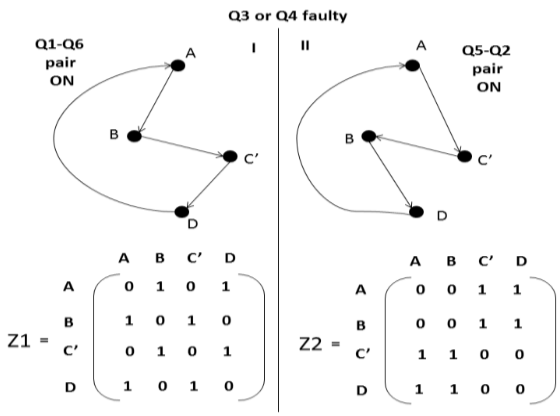
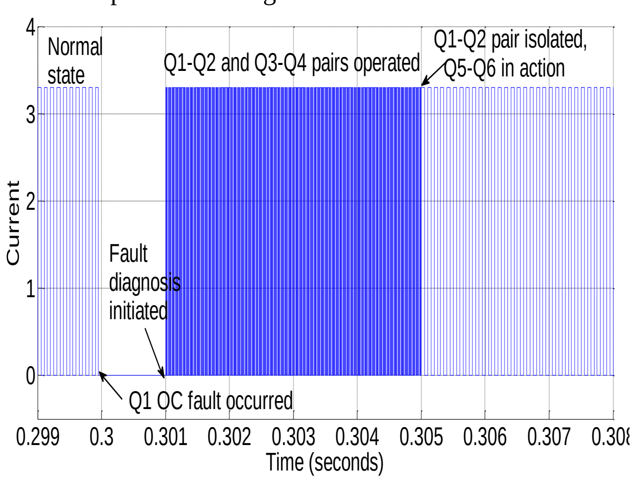


Fig. 6. Converter topology description in Q3 and Q4 fault recovery state

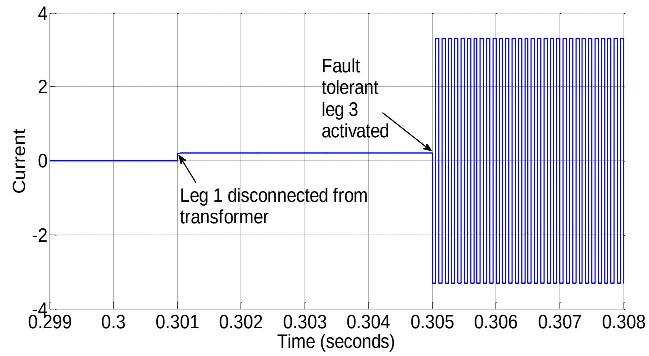
From graphs and the matrices shown in fig.4,5,6 it can be seen that when branch with faulty transistors is discarded and fault tolerant branch 3 is operated , the converter topology is same as original full bridge DC/DC converter topology. This shows that the converter efficiency and power remains the same.

B. Simulation results

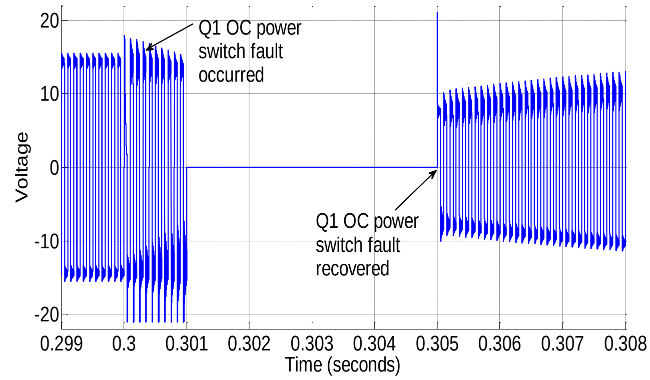
In this section simulation result of the proposed scheme are presented. Converter model is developed in which open power switch faults are automatically generated by disabling gate pulses [6], the controller automatically diagnoses open faulty power switch and activates fault tolerant branch. Results obtained in each power switch fault case are shown below. Current pulses at test points, relays and voltage pulses at transformer secondary and output in different open power switch faults are presented in figures 7 to 10.



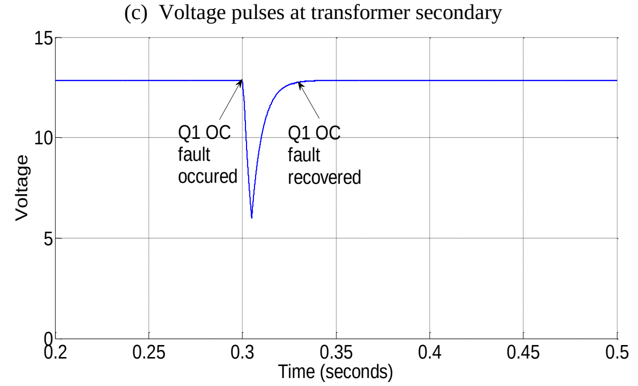
(a) Current pulses at test point TP2



(b) Current pulses at NO terminal of relay 1

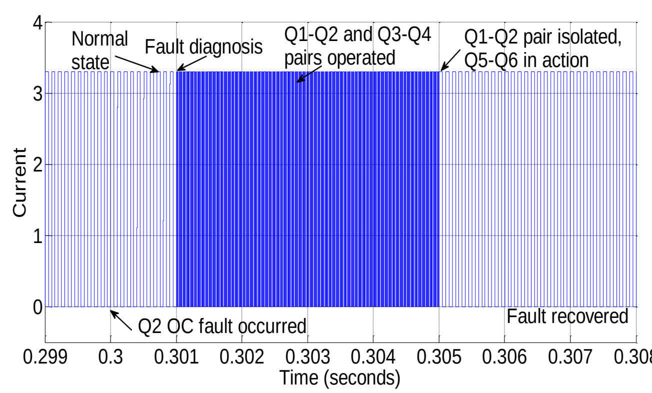


(c) Voltage pulses at transformer secondary

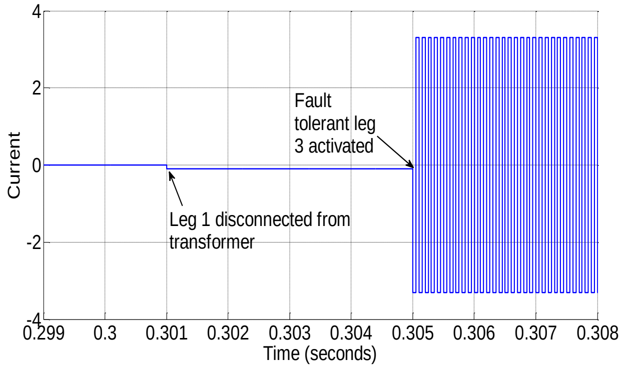


(d) Output voltage

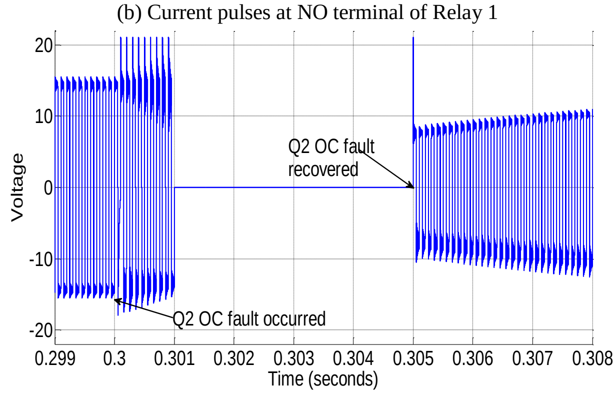
Fig.7. Waveforms at various nodes in normal state, Q1 OC faulty state, fault diagnosing state and in Q1 OC fault recovery state.



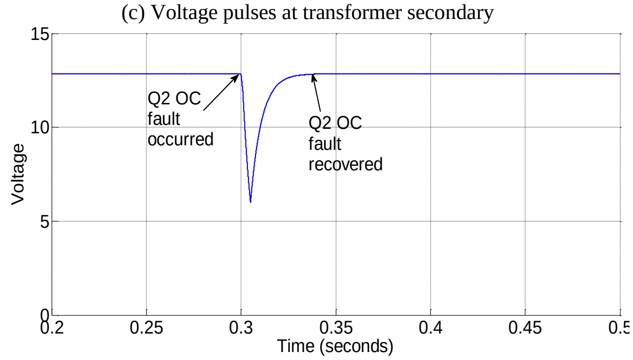
(a) Current pulses at TP2



(b) Current pulses at NO terminal of Relay 1

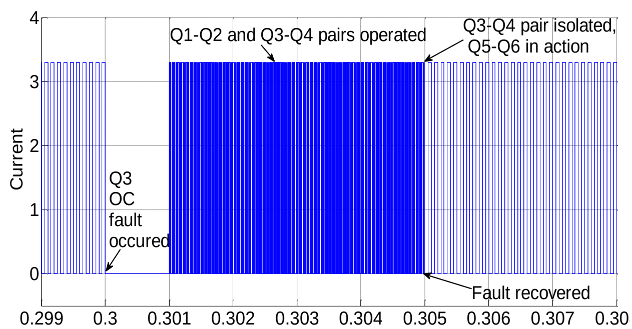


(c) Voltage pulses at transformer secondary

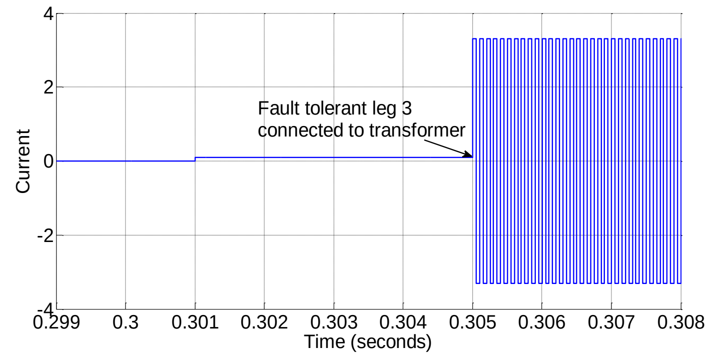


(d) Output voltage

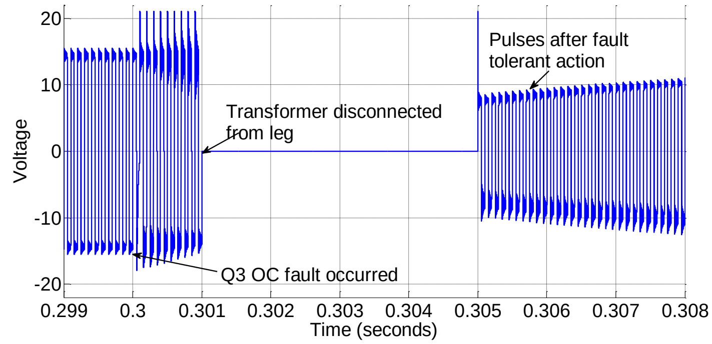
Fig. 8. Waveforms at various nodes in normal state, Q2 OC faulty state, fault diagnosing state and in Q2 OC fault recovery state.



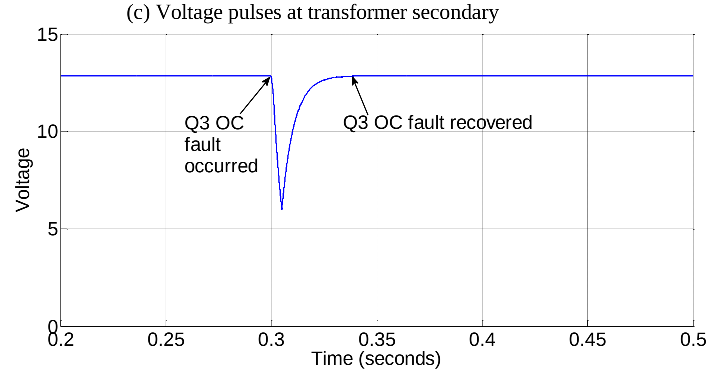
(a) Current pulses at TP1



(b) Current pulses at NO terminal of relay 2

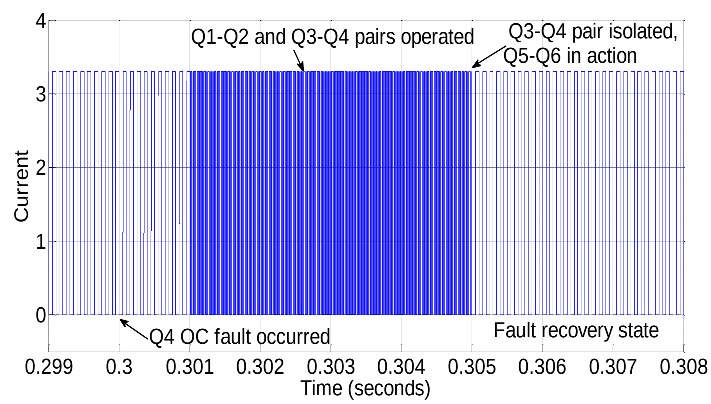


(c) Voltage pulses at transformer secondary

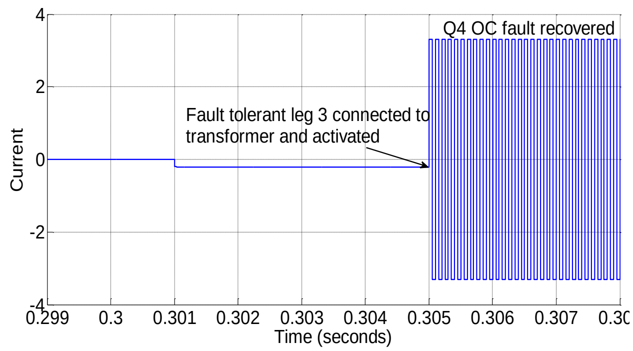


(d) Output voltage

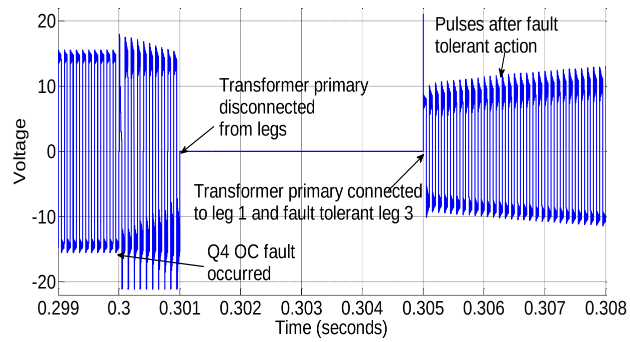
Fig. 9. Waveforms at various nodes in normal state, Q3 OC faulty state, fault diagnosing state and in Q3 OC fault recovery state.



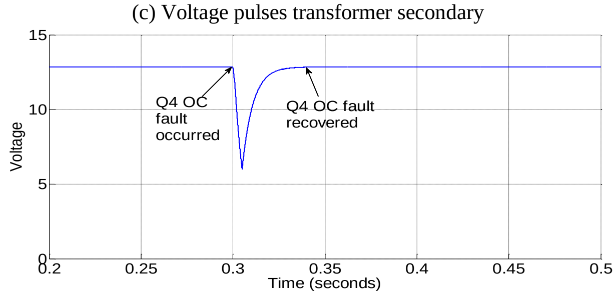
(a) Current pulses at TP1



(b) Current pulses at NO terminal of relay 2



(c) Voltage pulses transformer secondary



(d) Output voltage

Fig. 10. Waveforms at various nodes in normal state, Q4 OC faulty state, fault diagnosing state and in Q4 OC fault recovery state.

Simulation parameters are given in table 2.

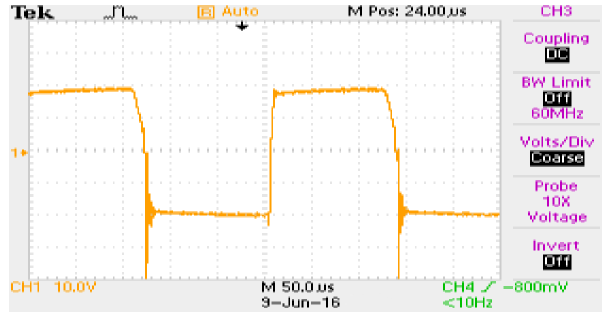
Table 2 System **s**imulation parameters

Parameter	Value
PV Voltage	21V
PV Current	3.3A
Load resistor	3.93Ω
DC Output voltage	12.85 V
DC Output Current	3.27A
Switching frequency	10KHz
TP1 RMS current	2.33A
TP2 RMS current	2.33A
Duty Cycle	50%

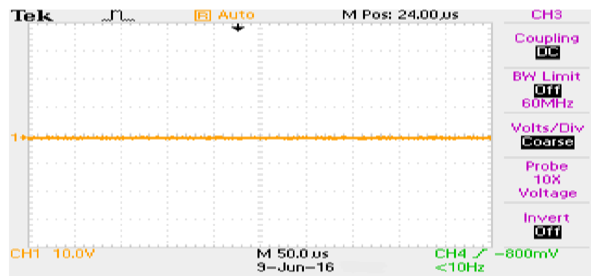
C. Experimental results

1. Q1 OCF diagnostic and tolerant control

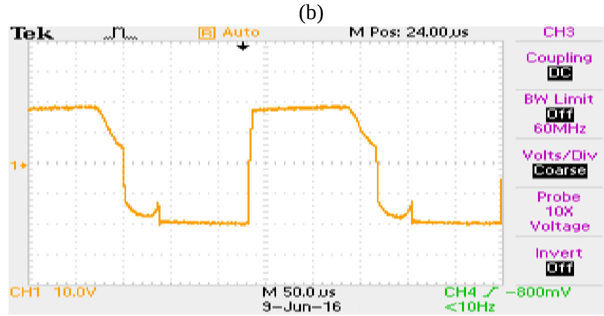
Arrival of Q1 open fault lowers current at test point TP2 which is considered as fault signature by controller. Fig.11. shows transformer primary voltage pulses.



(a)



(b)

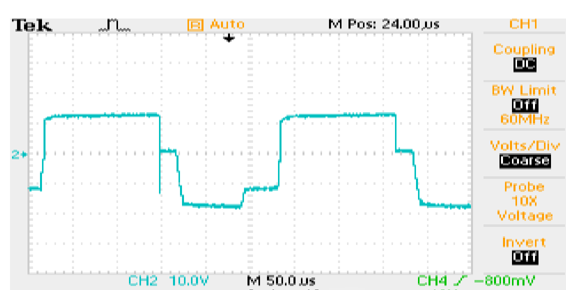


(c)

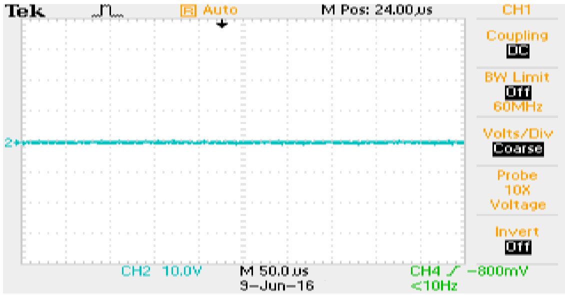
Fig. 11. Transformer primary voltage pulses in Q1 OC fault recovery process a) relay 1 and 2 at NC terminal b) relay 1 and 2 at NO terminal c) relay 1 at NO ; relay 2 at NC

2. Q2 OCF diagnostic and tolerant control

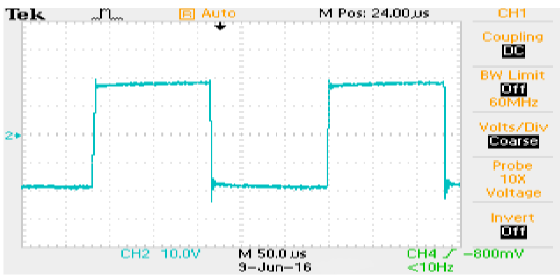
On arrival of Q2 open fault RMS current at TP1 decreases which is considered as fault signature. Fig.12 shows transformer primary voltage pulses.



(a)



(b)

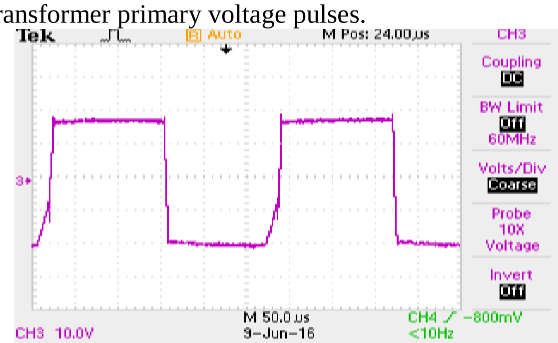


(c)

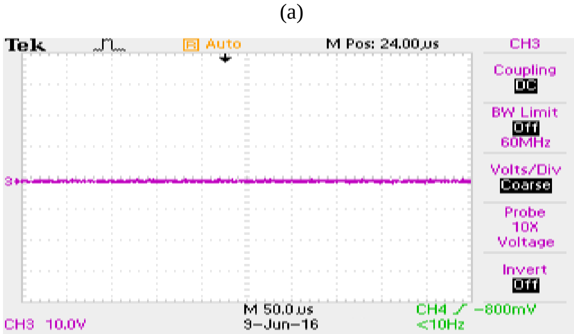
Fig. 12. Transformer primary voltage pulses in Q2 OC fault recovery process a) relay 1 and 2 at NC terminal b) relay 1 and 2 at NO terminal c) relay 1 at NO ; relay 2 at NC

3. Q3 OCF diagnostic and tolerant control

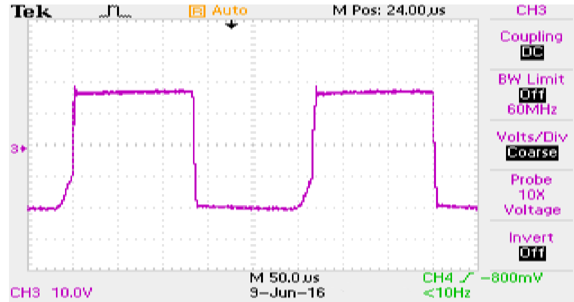
Q3 open switch fault generates fault signature at TP1, after detecting this fault signature, the controller circuitry switches relays to NO terminal. Fig.13 shows transformer primary voltage pulses.



(a)



(b)

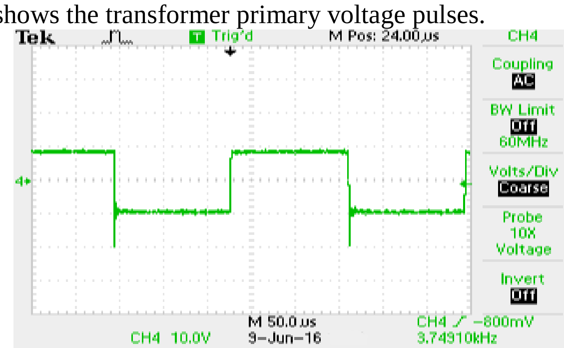


(c)

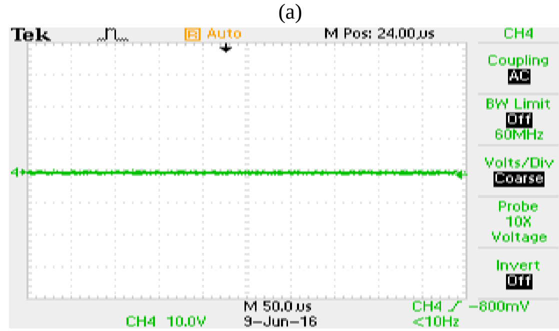
Fig. 13. Transformer primary voltage pulses in Q3 OC fault recovery process a) relay 1 and 2 at NC terminal b) relay a and 2 at NO terminal c) relay 1 at NC ; relay 2 at NO

4. Q4 OCF diagnostic and tolerant control

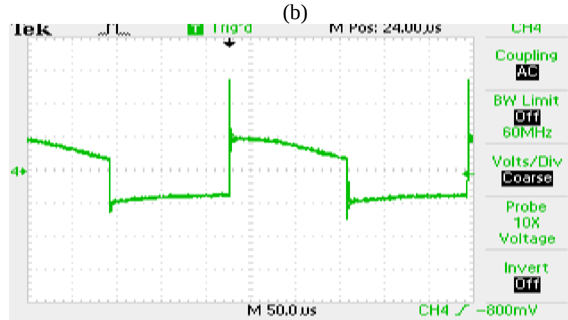
Q4 open fault decreases RMS current at TP2. Fig. 14 shows the transformer primary voltage pulses.



(a)



(b)



(c)

Fig. 14. Transformer primary voltage pulses in Q4 OC fault recovery process a) relay 1 and 2 at NC terminal b) relay 1 and 2 at NO terminal c) relay 1 at NC ; relay 2 at NO

Table 3- Normal state electrical parameters

Electrical parameter	Value
PV voltage (Instantaneous)	20.68V
PV current (Instantaneous)	2.4A
TP1 RMS current (normal state)	1.69A
TP2 RMS current (normal state)	1.69A
Transformer primary voltage	20Vpeak
Transformer secondary voltage	19Vpeak
Converter output current	1.91A
Converter output voltage	12.64V

In fault diagnosis state power switches in both branches are operated with same frequency and phase, hence both branches provides low impedance path and carries current resulting in short of the DC source, therefore this scheme is more convenient for use in photovoltaic application.

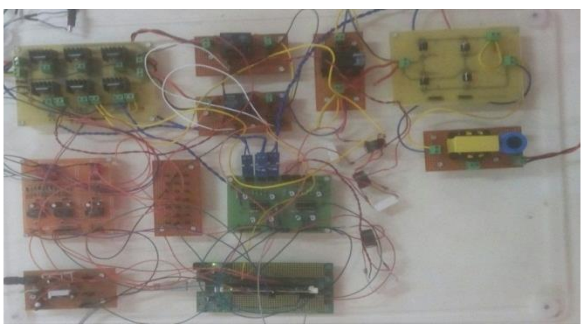


Fig. 15. Laboratory prototype

The merits of the scheme and technique presented in this research work are 1) automatic localization of exact faulty power switch and fault recovery within three seconds 2) no need of manual intervention and everything is done automatically 3) time needed for exact fault diagnosis and repair action is reduced to only three seconds (typically this time depends upon site location, component availability etc.) 4) the power levels in normal working state and fault recovery states are same, i.e. no loss of power 5) very few number of additional devices are required (two relays and two power switches), hence the solution is economical because the investment cost of entire PV system is very higher compared with the cost of additional devices. 6) fault is automatically recovered within few seconds hence power generation continues and loss due to temporary halt of power is also reduced. Thus the system is economical and any cost spent on additional components can be recovered from continual energy generation and hence revenue generation in spite of presence of faulty component. The drawback is need of high quality relays providing lower ON state resistance, long durability and precise relay control. The scheme and technique presented in this research work is applicable for the solar PV arrays installed at remote locations and which occupies the land areas in hectare.

5. Conclusions

The equivalence in matrices X1=Y1=Z1 and X2=Y2=Z2 in graph theory shows that the converter functionality in cycles 1 and 2 in normal state and in fault recovery state is similar; this shows the topological equivalence of converter in normal and faulty states. It reports the same efficiency and power in normal and fault recovery states. Simulation and experimental results have also shown that in recovery state system works with same power and efficiency as in normal state which is meritorious. Further fault is diagnosed and recovered automatically. Time taken from fault diagnosis to recovery state is approximately equal to relay switching time. By using this control scheme, single faulty switch from any branch and two faulty switches from single branch can be localized and fault can be recovered. The scheme is able to exactly locate faulty power switch. Since little number of components is required, proposed scheme is economical to implement. It can be applied to FBDCDC converter with and without center tapped transformers. It is applicable to soft switching control schemes with little modification. It is recommended to select relays of higher reliability. The scheme can be applied at remote PV power generation systems or at critical applications where occurrence of open power switch fault malfunction the system.

References

[1] Giovanni Petrone, Spagnuolo, Remus, Mummadi, Massimo, "Reliability issues in photovoltaic power processing systems", IEEE transactions on Industrial Electronics, Vol.55 No. 7, pp. 2569-2580, 2008.

[2] N.G.Dhere, "Reliability of PV modules and balance of system components", in proceedings of 31st IEEE photovoltaic Specialist. Conference., pp.1570-1576,2005.

[3] Hugo Callega, Freddy Chan, Israel Uribe, "Reliability oriented assessment of a DC/DC converter for photovoltaic applications", IEEE power electronics specialists conference, pp.1522-1527, 2007

[4] Shaoyang Yang, Angus Bryant, Philip Maybap, Dawei Xing, Peter Tanver, " An industry based survey of reliability in power electronics converters", IEEE transactions on industry applications, Vol. 47 No.3, pp. 1441-1451, 2011.

[5] Eunice Ribeiro, Antonio J. Marques Cardoso, Chiara Boccaletti, "Fault tolerant strategy for a Photovoltaic DC-DC converter", IEEE transactions on power electronics, Vol. 28 No. 6, pp.3008-3018, 2013.

[6] Xuejun Pei, Songsong Nie, Yu Chen, Yong Kang, "Open circuit fault diagnosis and fault tolerant strategies for full bridge DC-DC converters", IEEE transactions on power electronics, Vol. 27 No. 5, pp.2550-2565, 2012.

[7] A.M. Airbella, G.G. Oggier, L.E. Piris-Botalla, C.A.Falco, G.O.Garcia, "Open transistors and diodes fault diagnosis strategy for

dual active bridge DC-DC converter", 10th IEEE/IAS international conference on industry applications (INDUSCON) , pp. 1-6, 2012.
[8] Rui Wu, Frede Blaabjerg, Huai Wang, Marco Liserre, Francesco Iannuzzo, "Catastrophic failure and fault tolerant design of IGBT power electronic converters- AN overview" 39th Annual conference of the IEEE Industrial Electronics Society, pp.507-513, 2013
[9] Khalid Ambusaidi, Volkar Pickert, Bashar Zahawi, "New circuit topology for fault tolerant H-bridge DC-DC converter", IEEE transactions on power electronics,Vol. 25 No.6, pp. 1509-1516, 2010.
[10] Lu D.D.C, Soon J.L. Verstraete D., "Two transistor step down DC-DC converters with fault tolerant capability", Australian universities Power Electronics Conference, pp.1-5, 2014
[11] John Long Soon, Dylan Dah-Chuan Lu, "A simple open circuit fault detection method for a fault tolerant DC/DC converter" in proceedings of IEEE 11th International conference on Power Electronics and Drives Systems, Australia, 2015.
[12] S. Siouane, S. Jovanović, P. Poure and E. Jamshidpour, "An Efficient Fault Tolerant Cascaded Step-Up Step-Down Converter for Solar PV Modules," 2018 IEEE International Conference on Environment and Electrical Engineering and 2018 IEEE Industrial and Commercial Power Systems Europe (EEEIC / I&CPS Europe), Palermo, 2018, pp. 1-5.
[13] Ehsan Jamshidpour, Philippe Poure, Shahrokh Saadate, "Photovoltaic systems reliability improvement by real time FPGA based switch failure diagnosis and fault tolerant DC-DC converter", IEEE transactions on Industrial Electronics, Vol. 62 No.11, pp. 7247-7255, 2015.
[14] Xuejun Pei, Songsong Nie, Yong Kang, "Switch short circuit fault diagnosis and remedial strategy for full bridge DC-DC converters", IEEE transactions on power electronics, Vol. 30 No. 5, pp.996-1004, 2015
[15] Songsong Nie, Xuejun Pei, Yu Chen, Yong Kang, "Fault diagnosis of PWM DC-DC converters based on magnetic component voltage equation", IEEE transactions on power electronics, Vol. 29 No. 9, pp. 4978-4988, 2014.
[16] Ehsan Jamshidpour, Philippe Poure, Eskandar Gholipour, Shahrokh Saadate, "Single switch DC-DC converter with fault tolerant capability under open and short circuit switch failures", IEEE transactions on power electronics, Vol. 30 No. 5), pp.2703-2712, 2015.
[17] Eunice Ribeiro, Antonio J.M.Cardoso, C.Boccaletti, "Open circuit fault diagnosis in interleaved DC-DC converters", IEEE transactions on power electronics,Vol. 29 No. 6, pp. 3091_02, 2014.
[18] Levy Costa, Giampaolo Buticchi, Marco Liserre, "A fault tolerant series resonant DC-DC converter", IEEE transactions on power electronics,Vol. 32 No. 2,pp.900_5, 2017
[19] Yantao Song, Bingsen Wang, "Survey on reliability of power electronic systems", IEEE transactions on power electronics, vol. 28, no. 1, , pp. 591_04, January 2013
[20] Shaoyong Yang, Dawei Xiang, Angus Bryant, Philip Mawby, Li Ran, Peter Tavner, "Condition monitoring for device reliability in power electronic converters: A review", IEEE transactions on power electronics, Vol. 25, No.11, pp.2734_52, 2010
[21] Huai Wang, Frede Blaabjerg, Ke Ma, Rui Wu, "Design for reliability in power electronics in renewable energy systems – status and future", Fourth International Conference on Power Engineering, Energy and Electrical Drives (POWERENG),pp.1846-1851, 2013
[22] Alejandro D. Domınguez-Garcia, Philip T. Krein, "Integrating reliability into the design of fault tolerant power electronics systems", IEEE power electronics specialists conference, pp. 2665_71, 2008.
[23] Hugo Calleja, Freddy Chan, "Reliability: A neglected topic in the power electronics curricula", Journal of power electronics, Vol. 10, No.6.pp.660_66, Nov. 2010
[24] Huai Wang, Marco Liserre, Frede Blaabjerg, "Toward reliable power electronics-Challenges, design, tools and opportunities", IEEE Industrial Electronics Magazine,.pp.17-26, June 2013
[25] Yiqing Lian, D.Holliday, S.Finney, "Modular input parallel output series DC/DC converter control with fault detection and redundancy", IEEE Energy conversion congress and exposition, pp.3495_01, 2015,
[26] Kiwoo Park, Zhe Chen, " Open circuit fault detection and tolerant operation for a parallel connected SAB dc-dc converter", 29th Annual IEEE applied power electronics conference and exposition (APEC) March 2014, pp. 1966-1972.
[27] Deshang Sha, Zhiqiang Guo, Xiaozhong Liao, "Digital control strategy for input series output parallel modular DC/DC converters", Journal of Power Electronics, Vol. 10 No. 3, pp. 245-250, May 2010.

Dr. Shamkumar B. Chavan

Presently working as Assistant Professor at Department of Technology, Shivaji University ,Kolhapur, his research interests are renewable energy systems, embedded systems, VLSI design and power electronics. He has more than 16 years of industrial, teaching and research experience. He has filed two patents. He has published research papers in many reputed international journals and conferences.

Dr. Mahesh S. Chavan

Presently working as Professor and Dean at KIT's college of Engineering, Kolhapur. He obtained his Ph.D degree in biomedical signal processing from Kurukshetra University, India. He has more than 25 years of experience in teaching and research. He has published research papers in reputed journals and has filed two patents; he has chaired and has been called for invited talks in international conferences. He is adviser and has acted as referee for many national, international conferences. He has guided Ph.D scholars in research work. His areas of interest and expertise are VLSI, Digital Signal Processing, Biomedical Signal Processing and Power Electronics.