Counter-Based and MUX-Based Design of DPLL, a Comparative Study

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Abstract: ***The design of modern day communication system emphasizes on transmission and proper reception of data at minimum possible error rates and also at the same time on maintenance of high degrees of precision. But there are additional factors that add to it such as the operating speeds of the communication device developed should be compatible with the other sub-systems of the setup. Also, the design complexity of the device and the cost of design should be minimum. So, based on the various factors as mentioned above, a situation arises where a number of designs can be put forward for the same device having their sets of merits and demerits. As such, an analysis of these different designs is essential to derive an optimal solution which is the main objective of this work. Considering the various constraints at hand, we would like to put forward a comparative study between two different designs of the communication receiver device DPLL, namely the counter based DPLL and Multiplexer based DPLL design which brings to light the merits of one design over the other in terms of key parameters such as speed, design, complexity, hardware requirement etc.***

Keywords: Multiplexer, oscillator, detector, phase, recovery

1. Introduction

A Phase Locked Loop (PLL) is a control system that tries to generate an output signal whose phase is related to the phase of the input reference signal. It is an electronic circuit consisting of a voltage controlled oscillator and a phase detector [1]. This circuit compares the phase of the input signal with the phase of the signal derived from its output oscillator and adjusts the frequency of its oscillator to keep the phases matched [2]. DPLL is a digital version of analog PLL. The constituent parts of the DPLL are digital phase detector, digital loop filter and feedback element. Digital phase detector could be realized using X-OR gate or J.K. Flip-Flops and digital loop filter could be designed using fundamental filter design procedures. The feedback element present in DPLL is the discretized voltage controlled oscillator (VCO), also called digitally controlled oscillator (DCO) or numerically controlled oscillator (NCO) [3]. This feedback element generates the input reference signal and the phase detector detects the difference in phase of the incoming signal and the reference signal. The DPLL thus corrects and locks the phase of incoming signal and the reference signal and due to these the frequencies are also locked giving a replica of the original message pulse but with much improved noise performance and less design complexity at the output.

2. Theoretical Background

A traditional PLL control system comprises of analog elements such as phase detectors built up around signal multipliers, frequency eliminators realized with analog low pass or band pass elements and feedback loop formed by widely used frequency modulator VCO. The DPLL system, however, is more of a contemporary design, and built around digitized or partly analog and partly digitized components; the phase detector is built around an Ex-OR logic and loop filter for the first order system is a buffer amplifier. The critical part of the design, however, is the feedback oscillator and decides the overall performance of the system. Different design procedures can be used for it such as discretized VCO, Counter based design, Multiplexer based design etc. Based on the above discussion, the theoretical models for our designs have been elaborated below:

Counter-Based DPLL

The block diagram of Counter Based DPLL is shown in

Figure 1.

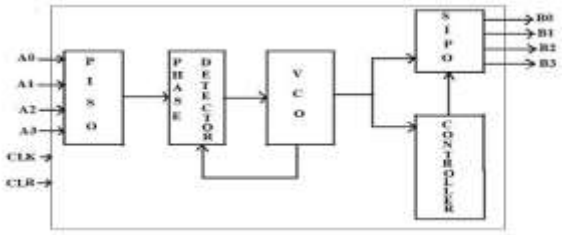

Figure 1: Block Diagram of Counter-Based DPLL

The first part of Counter Based DPLL is Parallel In Serial Out which gives output of one bit with respect to the clock. The second part is the Phase Detector which is realized using XOR logic to detect the phase difference between the input and the reference signal. The third part is the Voltage Controlled Oscillator which is realized with Counter and its task is to generate the same bit as that of the input bit. The fourth part is the Controller which locks the whole system once the message signal is out. The last part is the Serial in Parallel Out which outputs all the data with respect to the clock.

MUX-Based DPLL

The block diagram of MUX Based DPLL is shown in Figure 2.

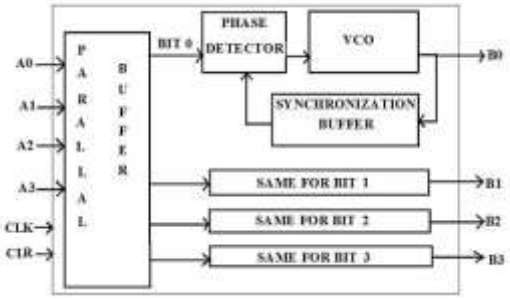

Figure 2: Block Diagram of MUX-Based DPLL

3. Literature Survey

There are various researches carried out by various researchers for the design of DPLL. Some of the researches carried out by them are presented in this section. The design of second order DPLL with uniformly sampled input and amplitude insensitive phase detector in which the design of DPLL is emphasized on the accuracy of output phase and improved performance at high values of gain [4]. The research is also carried out for the design of DPLL in 0.5µm CMOS process. In this design of DPLL the focus is mainly on the use of HDL platforms in order to get a proper logic design and also carried out CMOS level analysis for effective layout of the process [5]. The next research is the design of ADPLL in 0.25µm CMOS technology. In this design of ADPLL, the locking is achieved about 100 reference clock cycles [6]. The design of ADPLL is implemented in FPGA based on popular sequential circuits [7]. Similar kinds of work is found in [8][9].

4. Working Model

A number of designs have been proposed in recent times for designing of the contemporary PLL or the DPLL. The most important design aspect is the design of the feedback oscillator as it determines the overall performance of the device. Here, we have made a comparison between two designs; the first one aims at designing the oscillator with a synchronous counter and uses the LSB bit for the phase correction process; the second one aims at obtaining a very simplified combinational design and uses a simple 2:1 MUX for the feedback oscillator. The details of both the designs have been provided below:

Counter-Based DPLL

The name Counter Based is given because a counter based logic is used for the design of VCO. The circuit level diagram of Counter Based DPLL is shown in Figure 3.

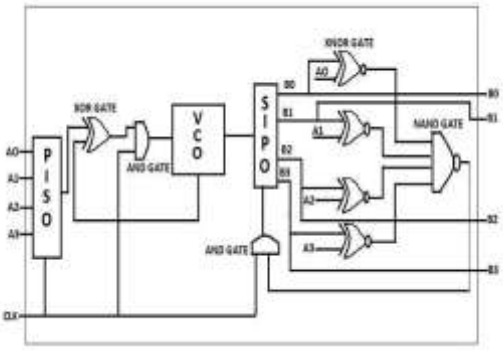

Figure 3: Counter-Based DPLL

The block wise explanation of Counter based DPLL is given below:

- The first block is parallel in serial out (PISO) shift register. It is designed in such a way that for an input data bit stream say for four bit, the first bit is faded to the DPLL at one clock. The second bit is faded to the DPLL at the next subsequent clock and so on. So PISO is used so that the message signals do not come in burst to the DPLL.

- The second block is the phase detector which is used to detect the phase between the input and the reference signal. The phase detector is designed using a XOR gate. When the input bit and the reference bit are same then the output of XOR gate is one else output is zero.

- The third block is the VCO. But before discussing VCO, we have used an AND whose inputs is the output of XOR gate and the master clock. The purpose of using AND gate is to control the operation of VCO. When the output of XOR gate is one i.e. the the input bit and the reference bit are not same then only the VCO will be activated. VCO is designed using counter based logic. The task of VCO is to generate the same bit as that of the input bit.

- The fourth block is serial in parallel out (SIPO) through which the output is obtained parallely.

- The small circuit comprises the Controller block. It is used to lock the whole system and realized using the basic combinational gates. After obtaining the output each output bit is checked to the input bit using XNOR logic. When it matched the output of XNOR gate will be one or else it will give zero. When all the bits are matched the output of XNOR will be one and hence the output of NAND gate is zero and the output of NAND gate is connected to AND gate and so the output of AND gate is zero and the SIPO will be deactivated and the clock signal is recovered.

MUX-Based DPLL

The name MUX Based is given because Multiplexer is used for the design of VCO. The circuit level diagram of MUX based DPLL is shown in Figure 4.

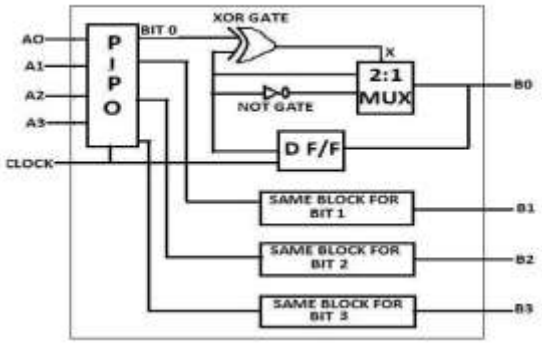

Figure 4: MUX-Based DPLL

The block wise explanation of MUX based VCO is given below:

- The first block is parallel in parallel out (PIPO) shift register which feds the whole input data stream to the DPLL.
- The second block is the phase detector and the same logic is used for this design as that of counter based DPLL.
- A 2:1 Multiplexer is used for the design of the third block which is the VCO. It generates the same bit as that of the input bit. The output of the MUX is initially zero. If the input bit is one there will be mismatch so the output of XOR gate is one (x=1) and the second line will be selected. The next time when it goes to the phase detector it will be matched and we get the output bit.
- D flip-flop is used for synchronization between input and the reference signal.
- For the remaining bits the same operation is going parallelly.
- The clock signal is finally recovered from the VCO.

5. Results and Discussions

Counter-Based DPLL

The schematic diagram of Counter-based DPLL is shown in figure 5.

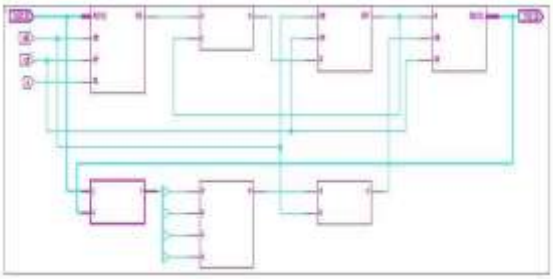

Figure 5: Schematic Diagram of Counter-Based DPLL

Figure 5, as can be seen above represents the RTL schematic layout generated for the proposed design of the DPLL device from hardware simulation. It depicts the various building blocks and how they are assembled together to make the DPLL receiver recover the original clock pulse from the corrupted input data accepted by it. A(0,3) is a four-bit vector which represents the corrupted received pulse. These four bits are simultaneously processed with the help of the Parallel-In Serial-Out(PISO) buffer which feds the data serially to the DPLL. The combinational block with two inputs is an Exclusive-OR based phase detector which determines whether the incoming data bits are in phase or out of

phase with the reference bits generated. The reference bits are generated by the VCO which is designed using counters and thus the name Counter based DPLL. The reference bits are feedback to the phase detector and when the input and the reference bit matched the output of XOR logic is zero and the clock signal is recovered from the VCO. A small controller circuit is used because for a four bit data stream we should recover the input bits after the fourth clock and it should remain as it is for the rest of the clock. But we have seen after the fourth clock the bits fluctuate which should be avoided. So we have used a small controlled circuit to overcome this problem.

The output waveform of counter-based DPLL is shown in figure 6

Figure 6: Output Waveform of Counter-Based DPLL

Figure 6, as shown above, represents the timing diagram generated for the proposed design. The figure shows A(0,3) which is a four- bit vector representing the input data set which is the corrupted data. Each component of the vector i.e. A(0), A(1) etc are shown as individual waveforms plotted against time. Similarly, B(0,3) is the four-bit vector which represents the recovered data or clock at the output of the VCO. The whole device operates on a single master clock which is depicted by the input to the system named as 'clk'. The DPLL captures or recovers the data during the time duration of the clock pulse or the duration of time for which 'clk' is '1'. For the proposed design, PISO is used for recovering each bit of the four-bit data with four clock pulses. So, for the n^{th} clock pulse, if a particular data say '1001' is recovered then in the subsequent n clock pulse. After the fourth clock pulse we obtained the final result and for the rest of the clock the data remained unchanged.

MUX-Based DPLL

The schematic diagram of MUX Based DPLL is shown in Figure 7.

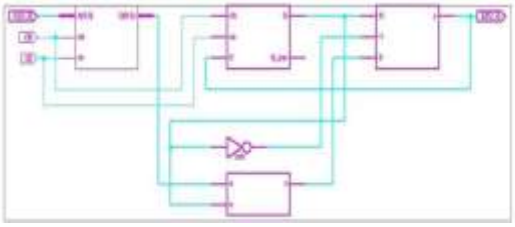

Figure 7: Schematic Diagram of MUX-Based DPLL

Figure 7 represents the RTL schematic diagram for the proposed design of MUX based DPLL. The RTL schematic depicts the various building blocks and their assemble to make the DPLL receiver recover the original clock pulse from the corrupted input data accepted by it. A(0,3) is a four-bit vector which represents the corrupted received pulse. These four bits are simultaneously processed with the help of the Parallel-In Parallel-Out(PIPO) buffer which synchronizes the incoming data bits with the main circuitry used for processing. The first block with two inputs is an Exclusive-OR based phase detector which determines whether the incoming data bits are in phase or out of phase with the reference bits generated. The reference bits which are generated by the VCO is designed using 2:1 multiplexers and thus the name MUX based DPLL. The reference bits are feedback to the XOR gate and so to synchronize this feedback process the D-flip flop block is used. At the output of the VCO, the clock pulse is recovered as the output.

The output waveform of MUX based DPLL is shown in figure 8.

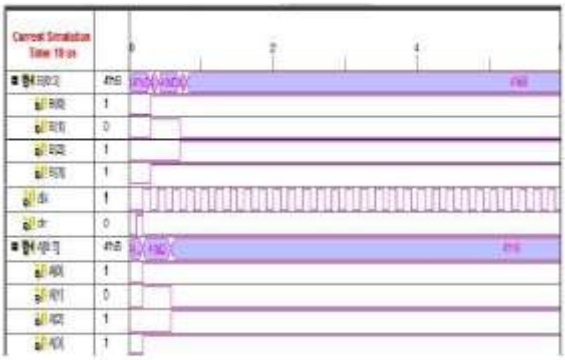

Figure 8: Output Waveform of MUX-Based DPLL

Figure 8 shows the timing diagram of MUX based DPLL. A(0,3) represents four bit input data which is the corrupted data. Similarly, B(0,3) represents the reference bits from the output VCO. . The whole device operates on a single master clock which is clk and DPLL recovers data during the duration of time for which clk is '1'. For the design of MUX based DPLL, parallel circuitry is used for recovering each bit of the four-bit data within a single clock pulse. So, for the n^{th} clock pulse, if a particular data say '1001' is recovered then in the subsequent $(n+1)^{th}$ clock pulse, a different data say '1100' can be recovered thus allowing the device to operate at very good speed.

After proper analysis of both the designs, i.e. the counter-based design and multiplexer-based design of the DPLL, a number of inferences can be drawn in terms

of speed, time complexity, design complexity, hardware requirement etc. They are stated as below:

- **Time:** For counter based DPLL system the time required for locking the incoming bits with the reference bits is more as compared to MUX based DPLL system because in counter based DPLL, it corrects only one bit at a time. For n bit data, the data will be locked at the end of n clock pulses. But in MUX based DPLL, parallel circuitry is used and hence data of any size can be locked at the end of a single clock pulse.

- **Complexity:** The counter based system uses a synchronous up counter as its primary component which is a complicated sequential design and hence increases the design complexity of the system. The multiplexer based system on the other hand uses a 2:1 MUX as its primary component and leads to simplification of design of the system because multiplexer is a comparatively simpler combinational logic. Thus, the multiplexer based system has lesser design complexity.

- **Hardware Requirement:** The counter based DPLL corrects one bit of data at a time and so it uses less hardware. The same hardware is used for all the bits by performing a parallel to serial data conversion at the input end. For enhanced speed, the multiplexer based design uses parallel circuitry, but in the process its hardware requirement increases. So, the hardware requirement for multiplexer based design is more.

- **Cost:** In terms of cost, the counter based design seems to be more cost-efficient as it uses lesser circuitry. But, actually for data of same size, the MUX based design is cheaper because it can be designed using very basic level circuitry at very less cost. Thus it is more cost efficient too.

- **Power Consumption:** Last but not the least, another important inference that we can draw is that the for the counter based design a controlled clock logic is used to ensure that locking action takes place only in case of a mismatch and also to keep the data locked once it is matched. This is done by masking the clock and thus in the process we save the clock from triggering the counter time and again leading to saving of clock energy. This complexity however has been removed in the multiplexer based design as it is able to lock the data at one clock pulse and keep it in locked state. However, here the clock energy is not saved due to continuous triggering. Thus, the counter based design is much more energy efficient.

6. Advantages and Limitations

Advantages of Counter-Based DPLL

- The hardware requirement of counter based DPLL is is less.
- Counter based design is more energy efficient as after all the bits are matched the controller block used in counter based DPLL will masked the clock pulse.

Advantages of MUX-Based DPLL

- The speed of MUX based DPLL is more.
- It is cost efficient.

Limitations of Counter-Based DPLL

- The design complexity of counter based DPLL is more.
- Speed of counter based DPLL is less.

Limitations of MUX-Based DPLL

- Less energy efficient as continuous triggering of clock pulse goes on even if all the input bits are matched. This is not significant when data is being sent at each clock pulse for matching. But, when the device is idle, it unnecessarily uses up the clock energy.
- Requires more amount of hardware.

7. Conclusion

After proper analysis and inferences from both design of DPLL, we can conclude that there is a tradeoff between speed and complexity of the circuit. We have seen MUX based DPLL is the most efficient approach as the speed is high and message signals can be send parallel. But this increases the complexity of the MUX based system which is overcome by counter based DPLL as it corrects only one bit at a time.

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