

Realization of Fractance Device using Continued Fraction Expansion Method

Battula Tirumala Krishna

Department of Electronics and Communication Engineering, University College of Engineering Kakinada,
Jawaharlal Nehru Technological University Kakinada (JNTUK),
Kakinada-533003, Andhra Pradesh, India.
tkbattula@gmail.com

Abstract: *The realization of fractional-order circuits is an emerging area of research for people working in the areas of control systems, signal processing and other related fields. In this paper, an attempt is made to realize fractance devices. The continued fraction expansion formula is used to calculate the fractance device's rational approximation. For the simulation in the experimentation, the third-order approximation for fractional order, $\alpha = -1/2, -1/3, -1/4$ is used. For the aim of mathematical simulation, the MATLAB platform was used. The proposed rational approximation is used to create a circuit. The TINA programme is used to simulate circuits. It has been discovered that the simulation and theoretical conclusions are in agreement.*

Keywords: Continued fraction expansion; Fractance device; Fractional order; Magnitude Response; Phase Response; Rational approximation; Simulation.

Open Access. Copyright ©Authors(s). Distributed under [Creative Commons Attribution 4.0 International License \(CC-BY\)](https://creativecommons.org/licenses/by/4.0/).
Article history- Received: 15 July 2021 and Accepted: 2 October 2021.

1. Introduction

Fractional Calculus is the branch of mathematics whose existence is found to be more than 300 years [1]. The main objective of this branch is dealing with the generalization of integration and differentiation to an arbitrary order, α . That means the integration and differentiation operations are generalized in Fractional Calculus. This mathematical concept finds applications in control systems, Instrumentation, Physics, Signal processing, Image processing, Electric Circuits, and other allied fields [2].

A fractional order differential equation is used to define a fractional order system. In the literature, it has been demonstrated that fractional order systems have an inherent attribute of limitless memory. For integer order systems, memory is limited. Fractional order systems include heat diffusion through solids, transmission lines, fractional order differentiators and integrators, and the nature of the hills.

Fractance device is an example of a fractional order system. This device is also called as constant phase element, fractor etc. The defining mathematical equation is, $Z(s) = \frac{k_0}{s^\alpha}$ where k_0 is a constant and s is a Laplace transform operator [3]. As the fractional order is changed, the behavior of the fractance device varies. For $\alpha = 0$ it behaves as a

resistor. It behaves as an inductor and capacitor as the value of α changes from -1 to $+1$. It functions as a Frequency Dependent Negative Resistor (FDNR) when the value is equal to 2 [2]. As a result, researchers are interested in the development of a fractance device.

Many different realization approaches are discussed in the literature. The first attempt to study the characteristics of the fractance is done by Sorimachi et.al. There are many procedures for calculating the rational approximation of fractance device. Every method has its advantages and disadvantages [4, 5, 6, 7, 8, 13]. Recent papers reveal the progress of the physical realization of the fractance device [14, 15, 16]. But it is not yet realized practically.

The goal of this study is to use the continued fraction expansion approach to create a fractance device. The circuit is constructed entirely of passive components. TINA software is used to test and plot the magnitude and phase responses of the proposed circuits.

The paper is divided into five sections. Section 2 contains a literature review. Section 3 explains the proposed methodology. Section 4 contains the findings and discussions. Finally, in section 5, the conclusions are presented.

2. Literature Survey

The creation of a fractance device is a long-standing and fascinating topic. For the realization, there are numerous approaches. Finding the rational approximation and realizing the calculated approximation are two of the approaches. Either passive or active aspects can be used in the realization. The capacitor functioning principle is the second method of realization. M. Nagakawa and K. Sorimachi [5] investigated the basic properties of the fractance device, in which they explored the analog realization of fractional controllers. The Nakagawa-Sorimachi circuit is a self-similar tree type circuit using resistors and capacitors [5].

Fractance devices can take the form of tree, chain, or net grid networks. In the literature, various recursive structural realizations have been presented [6, 7]. However, hardware complexity is a drawback [6, 7]. The cost of realization rises as the circuit complexity rises.

Calculation of the rational approximation is discussed by many researchers. Oustaloup approximation is predicated on the recursive distribution of zeros and poles [2, 3]. Carlson approximation is predicated on the regular newton process [7]. During this method, because the order increases, the value and complexity increase. The Matsuda methodology provides continuous approximations of fractional plants obtained by identifying a model from its gain. Suppose that the fractional order operator is to be approximated by $F(s)$. The gain must be determined at various frequencies, the number of which defines how many zeros and poles will be present in the approximation. $2M + 1$ frequencies must be utilized for M zeros and M poles. It's best to use an odd number of frequencies; if you use an even number, the number of zeros will equal the number of poles plus one, and the model will be improper [8].

This study proposes and uses a rational approximation based on the continued fraction expansion approach for the realization of fractance devices. This paper discusses the realization of third order rational approximation.

3. Proposed Method

In general, the differentiation and integration to the non-integer order are often represented by the operator, ${}_aD_t^\alpha$, where the variable ' α ' is the fractional order and ' p ' and ' t ' are the bounds of the operation. The fractional order differentiator/integrator in the time domain is defined [1] as:

$${}_pD_t^\alpha = \begin{cases} \frac{d^\alpha}{dt^\alpha} & \alpha > 0, \\ 1 & \alpha = 0, \\ \int_p^t (d\tau)^\alpha & \alpha < 0. \end{cases} \quad \dots (1)$$

The frequency domain representation of ideal differ-integrator with fractional order is $H(s) = (s)^{\pm\alpha}$ where ' α ' defines the fractional order and range of its value in between 0 to 1. The variable ' s ' equals to ' $j\omega$ ', where $\omega = 2\pi F$ radians/sec.

A fractional order system with input $x(t)$ and $y(t)$ is governed [9] by the following equation:

$$\begin{aligned} & a_n D^{\alpha_n} y(t) + a_{n-1} D^{\alpha_{n-1}} y(t) + \\ & a_{n-2} D^{\alpha_{n-2}} y(t) + \dots + \\ & a_0 D^{\alpha_0} y(t) = b_m D^{\beta_m} x(t) + \\ & b_{m-1} D^{\beta_{m-1}} x(t) + \dots + b_0 D^{\beta_0} x(t) \end{aligned} \quad \dots (2)$$

Where

$a_n, a_{n-1}, a_{n-2}, \dots, a_0$ and b_m, b_{m-1}, \dots, b_0 are system coefficients and the differentiation orders are integer multiple of based orders i.e., $\alpha_k = \beta_k = k\alpha$.

Applying the Laplace transform of equation (2) and setting the initial condition to zero, the transfer function is [9] :

$$\begin{aligned} H(s) &= \frac{Y(s)}{X(s)} \\ &= \frac{b_m s^{\beta_m} + b_{m-1} s^{\beta_{m-1}} + \dots + b_0 s^{\beta_0}}{a_n s^{\alpha_n} + a_{n-1} s^{\alpha_{n-1}} + \dots + a_0 s^{\alpha_0}} \end{aligned} \quad \dots (3)$$

The main advantage of fractional orders over integer order systems is their ability to use infinite memory. In integer order systems, memory is finite.

The generalized fractional differentiation and integration are used for determining the time integral and derivative of the given signal for any arbitrary order. Many definitions for calculating fractional orders are available in the literature. The two basic definitions of a fractional order difference integrator are Grunwald-Letnikov (G-L) and Riemann-Liouville (R-L) [1]. Grunwald-Letnikov (G-L) definition is,

$$D_t^\alpha f(t) = \lim_{h \rightarrow 0} \frac{1}{h^\alpha} \sum_{i=0}^{\infty} (-1)^i \binom{\alpha}{i} f(t - ih) \quad \dots(4)$$

Where

$$\binom{\alpha}{i} = \frac{\Gamma(\alpha + 1)}{\Gamma(i + 1) \Gamma(\alpha - i + 1)} \quad \dots(5)$$

where $\Gamma(\cdot)$ is Euler's gamma function.

Riemann-Liouville (R-L) definition is,

$${}_aD^p f(t) = \frac{1}{\Gamma(n-p)} \frac{d^n}{dt^n} \int_a^t \frac{f(\tau)}{(t-\tau)^{p-n+1}} d\tau \quad \dots (6)$$

for $(n - 1 < p < n)$, where a and t are the limits of the operation ${}_aD^p f(t)$.

A. N. Khovanskii [11] has proposed the continued fraction expansion as follows:

$$(1+x)^\alpha = \frac{1}{1 - \frac{\alpha x}{1 + \frac{1}{2} \frac{1}{1 - \frac{1}{6} \frac{1}{1 + \frac{1}{6} \frac{1}{1 - \frac{1}{10} \frac{1}{1 + \frac{1}{10} \frac{1}{1 - \frac{1}{14} \frac{1}{1 + \dots}}}}}}}}}} \quad \dots (7)$$

This continued fraction expansion is convergence in the finite complex s-plane from $x = -\infty$ to $x = -1$ and substitute x by $(s - 1)$ to obtain the expansion of s^α . Now, truncated to some finite number of terms and obtain FODs and FOIs for various fractional orders $\alpha = \frac{1}{2}, \frac{1}{3}$ and $\frac{1}{4}$ etc. Depending on the truncation order of CFE, the degree of denominator and numerator polynomials in the obtained rational transfer function have been changed.

Table 1: Rational Approximations for fractional order $\alpha = \frac{1}{2}, -\frac{1}{2}$

Rational Approximations for $s^{\frac{1}{2}}$ using CFE method	
Number of terms	Rational approximations
2	$G_{2-1/2}(s) = \frac{3s + 1}{s + 3}$
4	$G_{4-1/2}(s) = \frac{5s^2 + 10s + 1}{s^2 + 10s + 5}$
6	$G_{6-1/2}(s) = \frac{7s^3 + 35s^2 + 21s + 1}{s^3 + 21s^2 + 35s + 7}$
8	$G_{8-1/2}(s) = \frac{9s^4 + 84s^3 + 126s^2 + 36s + 1}{s^4 + 36s^3 + 126s^2 + 84s + 9}$
10	$G_{10-1/2}(s) = \frac{11s^5 + 165s^4 + 462s^3 + 330s^2 + 55s + 1}{s^5 + 55s^4 + 330s^3 + 462s^2 + 165s + 1}$
Rational Approximations for $s^{-\frac{1}{2}}$ using CFE method	
2	$H_{2-1/2}(s) = \frac{s + 3}{3s + 1}$

4	$H_{4-1/2}(s) = \frac{s^2 + 10s + 5}{5s^2 + 10s + 1}$
6	$H_{6-1/2}(s) = \frac{s^3 + 21s^2 + 35s + 7}{7s^3 + 35s^2 + 21s + 1}$
8	$H_{8-1/2}(s) = \frac{s^4 + 36s^3 + 126s^2 + 84s + 9}{9s^4 + 84s^3 + 126s^2 + 36s + 1}$
10	$H_{10-1/2}(s) = \frac{s^5 + 55s^4 + 330s^3 + 462s^2 + 165s + 1}{11s^5 + 165s^4 + 462s^3 + 330s^2 + 55s + 1}$

Table 2: Rational Approximations for fractional order $\alpha = \frac{1}{3}, -\frac{1}{3}$

Rational Approximations for $s^{\frac{1}{3}}$ using CFE method	
Number of terms	Rational approximations
2	$G_{2-1/3}(s) = \frac{2s + 1}{s + 2}$
4	$G_{4-1/3}(s) = \frac{14s^2 + 35s + 5}{5s^2 + 35s + 14}$
6	$G_{6-1/3}(s) = \frac{7s^3 + 42s^2 + 30s + 2}{2s^3 + 30s^2 + 42s + 7}$
8	$G_{8-1/3}(s) = \frac{91s^4 + 1001s^3 + 1716s^2 + 572s + 22}{22s^4 + 572s^3 + 1716s^2 + 1001s + 91}$
10	$G_{10-1/3}(s) = \frac{52s^5 + 910s^4 + 2860s^3 + 2288s^2 + 440s + 11}{11s^5 + 440s^4 + 2288s^3 + 2860s^2 + 910s + 52}$
Rational Approximations for $s^{-\frac{1}{3}}$ using CFE method	
2	$H_{2-1/3}(s) = \frac{s + 2}{2s + 1}$
4	$H_{4-1/3}(s) = \frac{5s^2 + 35s + 14}{14s^2 + 35s + 5}$
6	$H_{6-1/3}(s) = \frac{2s^3 + 30s^2 + 42s + 7}{7s^3 + 42s^2 + 30s + 2}$
8	$H_{8-1/3}(s) = \frac{22s^4 + 572s^3 + 1716s^2 + 1001s + 91}{91s^4 + 1001s^3 + 1716s^2 + 572s + 22}$
10	$H_{10-1/3}(s) = \frac{11s^5 + 440s^4 + 2288s^3 + 2860s^2 + 910s + 52}{52s^5 + 910s^4 + 2860s^3 + 2288s^2 + 440s + 11}$

Table 1 contains rational approximations of fractional orders $\alpha = 1/2, -1/2$. Table 2 and Table 3 shows a rational approach to using CFE for one-third and one-quarter differentiators and integrators, respectively.

Figure 1, 2 show the amplitudes and phase responses of the analog differentiator and integrator of half order respectively. Figures 1(a) and 2(a) are the magnitude responses and Figures 1(b) and 2(b) are phase responses. Figures 3-6 demonstrate the responses of the one-third and one-fourth fractional order differentiators and integrators. Figures 3(a), 4(a), 5(a), 6(a) are the magnitude responses for the orders 1/3, -1/3, 1/4, -1/4 respectively. Figures 3(b), 4(b), 5(b), 6(b) are the Phase responses for the orders 1/3, -1/3, 1/4, -1/4. From the figures, it is clear that the fifth-order rational transfer function matches the ideal response. As the order of the rational transfer function increases, the response approaches the ideal. However, the number of terms has increased, the hardware complexity has increased, and the cost has increased. Therefore, the optimal order value was selected to compromise both system performance and hardware requirements.

The magnitude responses show that when fractional order diminishes, the magnitude in dB lowers as well. The increase in dB is proportional to the fractional order of the differentiator. The half order, one-third, and one-fourth order differentiators have phases of 45, 30, and 22.50 degrees respectively, while the half order, one-third, and one-fourth order integrators have phases of -45, -30, and -22.50 degrees respectively. As a result, the phase angle of a fractional order differ-phase integrator's is defined as

$$Phase \text{ (in degrees)} = \pm\alpha * 90 \quad \dots (8)$$

In the above equation, + sign stands for differentiator and - sign for integrator.

Table 3: Rational Approximations for fractional order $\alpha = \frac{1}{4}, -\frac{1}{4}$

Rational Approximations for $s^{\frac{1}{4}}$ using CFE method	
Number of terms	Rational approximations
2	$G_{2_1/4}(s) = \frac{5s + 3}{3s + 5}$
4	$G_{4_1/4}(s) = \frac{15s^2 + 42s + 7}{7s^2 + 42s + 15}$
6	$G_{6_1/4}(s) = \frac{195s^3 + 1287s^2 + 1001s + 77}{77s^3 + 1001s^2 + 1287s + 195}$
8	$G_{8_1/4}(s) = \frac{663s^4 + 7956s^3 + 14586s^2 + 5236s + 231}{231s^4 + 5236s^3 + 14586s^2 + 7956s + 663}$
10	$G_{10_1/4}(s) = \frac{663s^5 + 12597s^4 + 41990s^3 + 35530s^2 + 7315s + 209}{209s^5 + 7315s^4 + 35530s^3 + 41990s^2 + 12597s + 663}$
Rational Approximations for $s^{-\frac{1}{4}}$ using CFE method	
2	$H_{2_1/4}(s) = \frac{3s + 5}{5s + 3}$
4	$H_{4_1/4}(s) = \frac{7s^2 + 42s + 15}{15s^2 + 42s + 7}$
6	$H_{6_1/4}(s) = \frac{77s^3 + 1001s^2 + 1287s + 195}{195s^3 + 1287s^2 + 1001s + 77}$
8	$H_{8_1/4}(s) = \frac{231s^4 + 5236s^3 + 14586s^2 + 7956s + 663}{663s^4 + 7956s^3 + 14586s^2 + 5236s + 231}$
10	$H_{10_1/4}(s) = \frac{209s^5 + 7315s^4 + 35530s^3 + 41990s^2 + 12597s + 663}{663s^5 + 12597s^4 + 41990s^3 + 35530s^2 + 7315s + 209}$

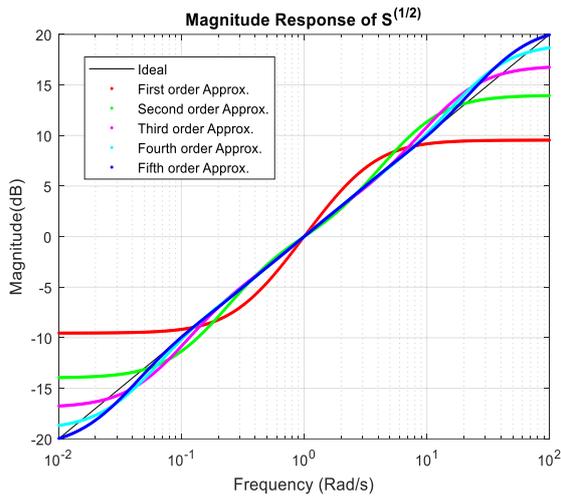


Figure 1(a)

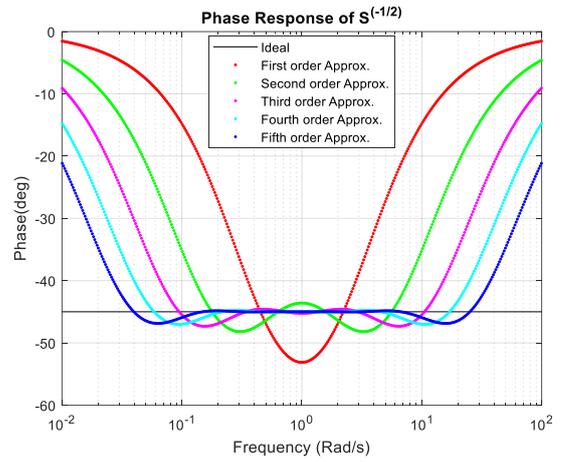


Figure 2(b)

Figure 2: (a) Magnitude (b) Phase response of analog half fractional order integrator

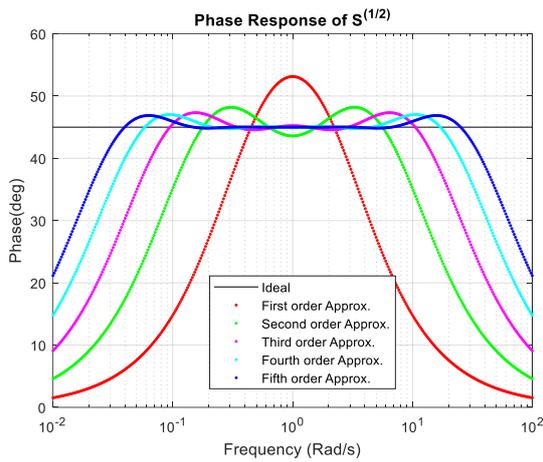


Figure 1(b)

Figure 1: (a) Magnitude (b) Phase response of analog half fractional order differentiator

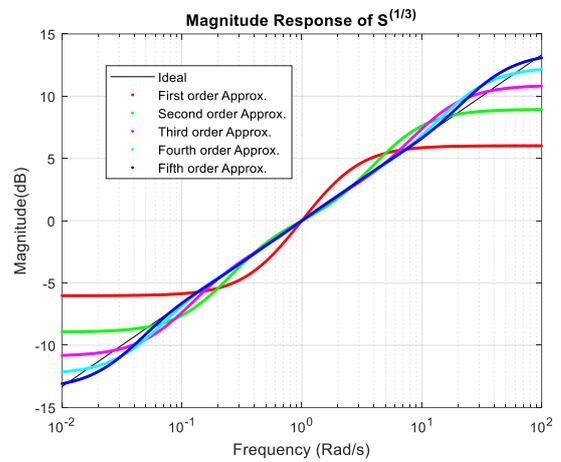


Figure 3(a)

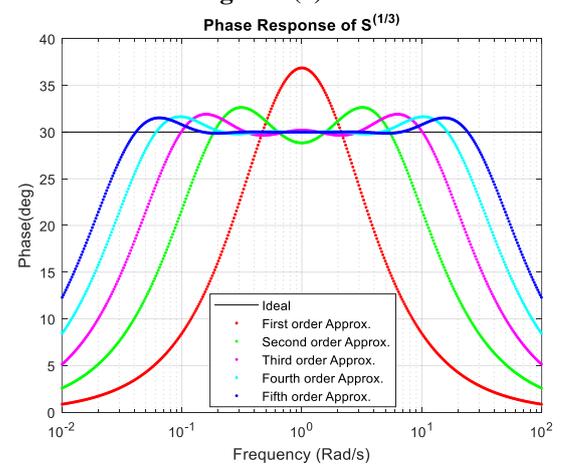


Figure 3(b)

Figure 3: (a) Magnitude (b) Phase response of analog one-third fractional order differentiator

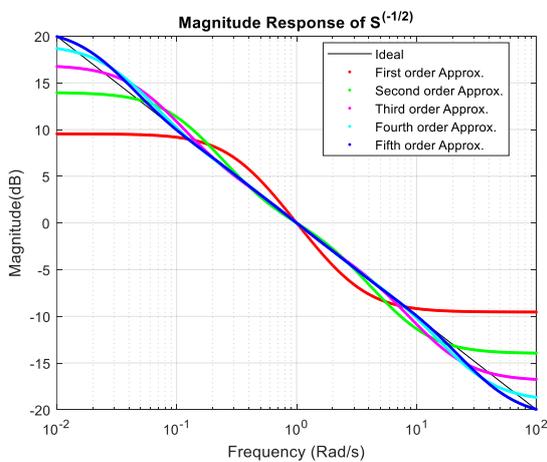


Figure 2(a)

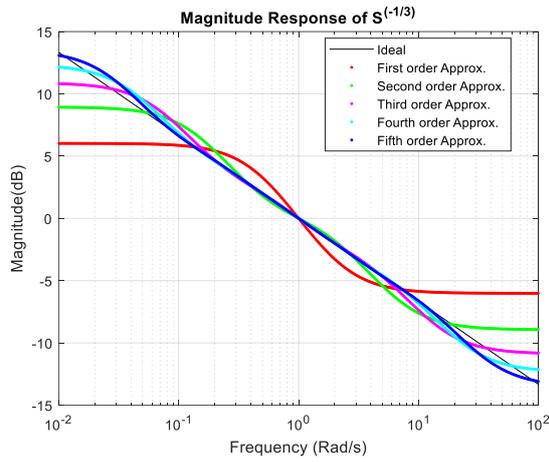


Figure 4(a)

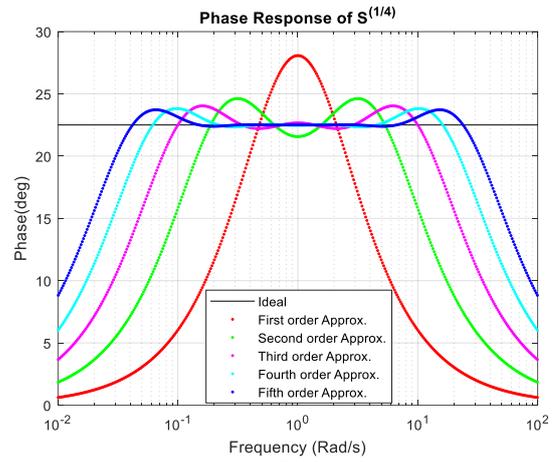


Figure 5(b)

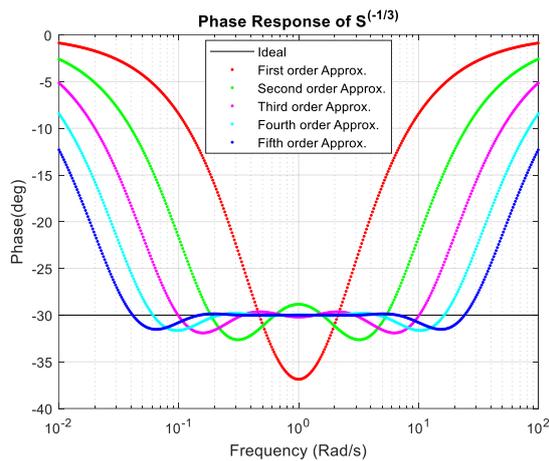


Figure (b)

Figure 4: (a) Magnitude (b) Phase response of analog one-third fractional order integrator

Figure 5: (a) Magnitude (b) Phase response of analog one-fourth fractional order differentiator

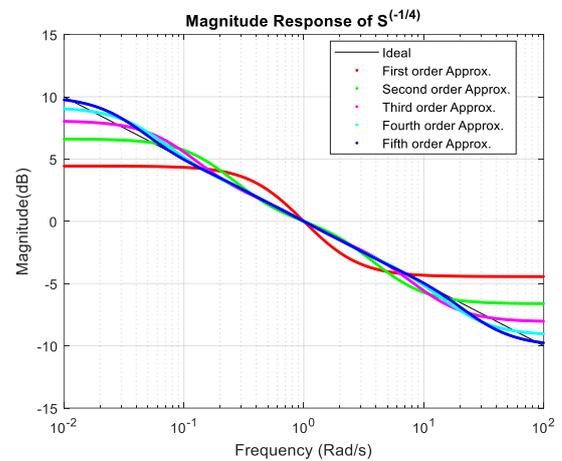


Figure 6(a)

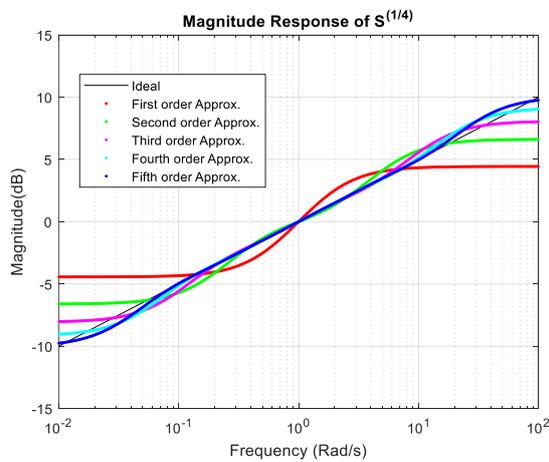


Figure 5(a)

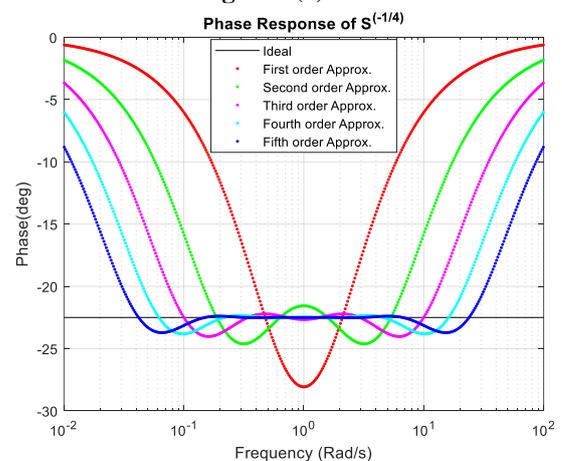


Figure 6(b)

Figure 6: (a) Magnitude (b) Phase response of analog one-fourth fractional order integrator

4. Results and discussions

The residue function of MATLAB is used to realize the third order rational approximation. It provides the partial expansion of the transfer function. The resistance and capacitance values are computed depending on the value of fractional orders 1/2, 1/3. For third-order approximation, the number of passive elements is 7, and the circuit appears as below in Figure 7 [12]. The values of the resistance and capacitance change depending upon the value of fractional order. Active realization of fractance device is shown in Fig.8. Fig.9 and 10 depict the results obtained for the application of sine and square wave signals ($\alpha = -0.5$). There is a delay in the sine wave response. Fig.11 and 12 are the input and output signals for the fractional order, $\alpha = -1/3$. The frequency under consideration is 100 mHz. To verify the efficacy of the proposed circuit, a bode plot is drawn as shown in Fig. 13 for $\alpha = -1/3$ case.

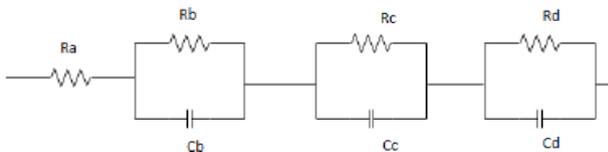


Figure 7: Passive circuit of fractance device

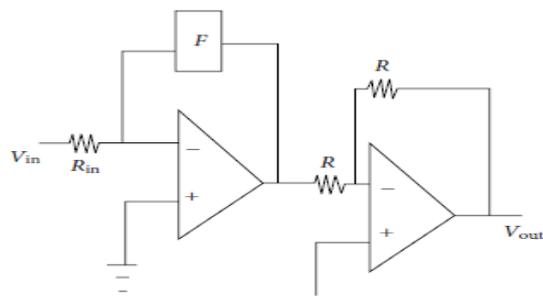


Figure 8: Realization of fractance device using operational amplifier

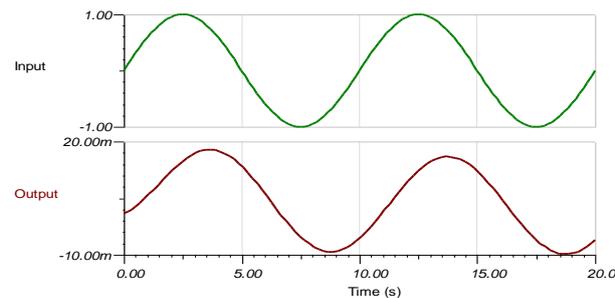


Figure 9: Input and output waveforms for 100 mHz sinewave (3rd order Approximation to $\alpha = -0.5$)

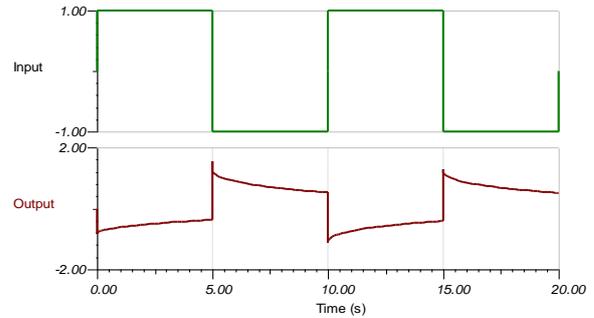


Figure 10: Input and output waveforms of square wave with Frequency 100 mhz (3rd order approximation to $\alpha = -0.5$)

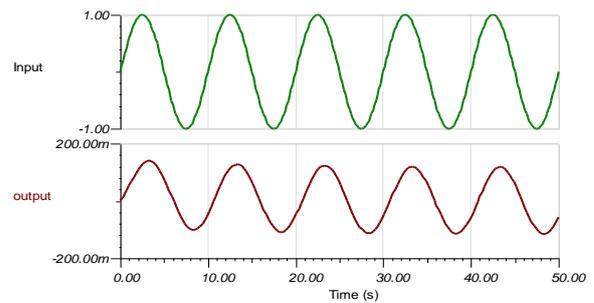


Figure 11: Input and output waveforms of sine signal with a frequency of 100 mHz ($\alpha = -1/3$)

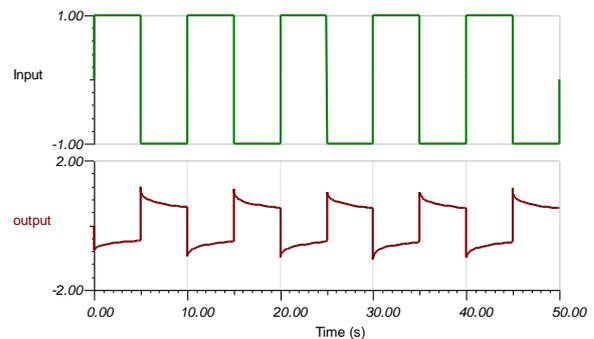


Figure 12: Input and output waveforms for $\alpha = -1/3$ at 100 mhz

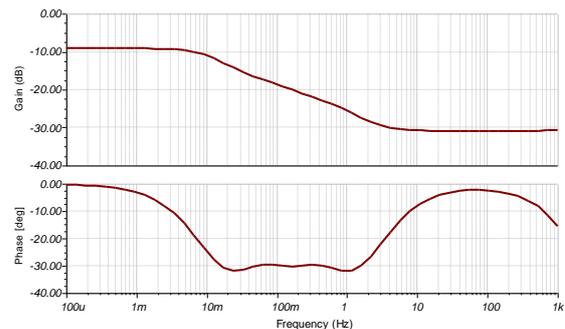


Figure 13: Bode plot of $\alpha = -1/3$ case

5. Conclusions

This work describes the realization of a fractance device of order $1/2$, $1/3$. The continued fraction expansion method is used to get the rational approximation. The order of the approximation is limited to third order due to the hardware complexity. The MATLAB residue function is used to create the third order approximation utilizing passive elements. Using an operational amplifier, active realization is achievable. The circuit simulations are carried out utilizing TINA software. The acquired results are closer to those predicted by theory. The frequency of the input signal is set to 100 mHz. Both square wave and sine wave are used as inputs, and the responses are recorded.

Acknowledgement

This work is carried out in support of the DST project SERB No. SB/FTP/ETA-048/2012 on dated 06-01-2017 being funded by the Department of Science and Technology (DST), Ministry of Science and Technology, Govt. of India. The author would like to thank the sponsorship agency for its support. The author also thanks the university authorities, Jawaharlal Nehru Kakinada Institute of Technology, Kakinada, Andhra Pradesh (India) for providing the necessary equipment to carry out this work.

References

- [1] K. B. Oldham and J. Spanier (Ed.), *The Fractional Calculus Theory and Applications of Differentiation and Integration to Arbitrary Order*, Elsevier, 1974.
- [2] B. T. Krishna, "Studies on fractional order differentiators and integrators: A survey," *Signal Processing*, vol. 91, no. 3, pp. 386–426, Mar. 2011, doi: 10.1016/j.sigpro.2010.06.022.
- [3] A. Yüce and N. Tan, "Electronic realisation technique for fractional order integrators," *The Journal of Engineering*, vol. 2020, no. 5, pp. 157–167, May 2020, doi: 10.1049/joe.2019.1024.
- [4] I. Podlubny, I. Petráš, B. M. Vinagre, P. O'Leary, and L. Dorčák, "Analogue realizations of fractional-order controllers," *Nonlinear Dynamics*, vol. 29, no. 1/4, pp. 281–296, 2002, doi: 10.1023/A:1016556604320.
- [5] M. Nagakawa and K. Sorimachi, "Basic Characteristics of a Fractance Device," in *IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences*, 1992, vol. E75-A, no.12, pp.1814–1819. [Online]. Available: https://search.ieice.org/bin/summary.php?id=e75-a_12_1814
- [6] P. Yifei *et al.*, "Structuring Analog Fractance Circuit for $1/2$ order Fractional Calculus," in *IEEE 2005 6th International Conference on ASIC*, Shanghai, China, 2005, vol. 2, pp. 1136–1139. doi: 10.1109/ICASIC.2005.1611507.
- [7] G. Carlson and C. Halijak, "Approximation of Fractional Capacitors $(1/s)^{(1/n)}$ by a Regular Newton Process," *IEEE Trans. Circuit Theory*, vol. 11, no. 2, pp. 210–213, 1964, doi: 10.1109/TCT.1964.1082270.
- [8] K. Matsuda and H. Fujii, "H(infinity) optimized wave-absorbing control - Analytical and experimental results," *Journal of Guidance, Control, and Dynamics*, vol. 16, no. 6, pp. 1146–1153, Nov. 1993, doi: 10.2514/3.21139
- [9] I. Podlubny, *Fractional-order systems and fractional-order controllers*, Institute of Experimental Physics, Slovak Academy of Sciences, Slovakia, Nov. 1994. [Online]. Available: <http://citeseerx.ist.psu.edu/viewdoc/download?doi=10.1.1.13.6602&rep=rep1&type=pdf>
- [10] A. A. Stanislavsky, "Twist of fractional oscillations," *Physica A: Statistical Mechanics and its Applications*, vol. 354, pp. 101–110, Aug. 2005, doi: 10.1016/j.physa.2005.02.033
- [11] A. N. Khovanskii, *The Application of Continued Fractions and Their Generalizations to Problems in Approximation Theory*, Netherlands: P. Noordhoff, 1963.
- [12] M. E. V. Valkenburg, *Introduction to modern network synthesis*, John Wiley and Sons, 1960.
- [13] B. T. Krishna and K. V. V. S. Reddy, "Active and Passive Realization of Fractance Device of Order $1/2$," *Active and Passive Electronic Components*, vol. 2008, Article ID 369421, pp. 1–5, 2008, doi: 10.1155/2008/369421.
- [14] A. Kartci, N. Herencsar, J. T. Machado, and L. Brancik, "History and Progress of Fractional-Order Element Passive Emulators: A Review," *Radioengineering*, vol. 29, no. 2, pp. 296–304, 2020.

- [15] A. Agambayev, *Design, fabrication and application of fractional-order capacitors*, PhD Thesis, Computer, Electrical and Mathematical Science and Engineering (CEMSE) Division, King Abdullah University of Science and Technology, Thuwal, Kingdom of Saudi Arabia, 2019. [Online]. Available: <http://hdl.handle.net/10754/631276>
- [16] Z. M. Shah, M. Y. Kathjoo, F. A. Khanday, K. Biswas, and C. Psychalinos, "A survey of single and multi-component Fractional-Order Elements (FOEs) and their applications," *Microelectronics Journal*, vol. 48, 2019. doi: <https://doi.org/10.1016/j.mejo.2018.12.010>

Author's Profile

Battula Tirumala Krishna, PhD, is a professor at the Jawaharlal Nehru Technological University Kakinada, Andhra Pradesh, India. In 2002, he graduated from Andhra University with a master's degree in electronics and communication engineering. He was an Associate Professor at Visakhapatnam's GITAM University previously. Fractional order systems and signal processing are two of his research interests. He is currently working on a DST project titled "Realization of Fractance Device" funded with an aid of Rs. 16.37 lakhs. He is a Chartered Engineer, FIETE-Fellow of Institution of Electronics and Telecommunication Engineers (IETE, India), as well as a FIE- Fellow of The Institution of Engineers (India).

